Reed Electronics Group

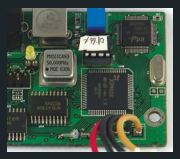
EDN

VOICE OF THE ENGINEER

MAY 11

Issue 10/2006

www.edn.com



DESIGNERS CAST A SKEPTICAL EYE ON MIXED-SIGNAL SOCs

Page 48

HAZARDOUS-VOLTAGE PRIMER

Page 39

SPREAD-SPECTRUM CLOCKING: measuring accuracy and depth

Page 61

Effective use of IC-amplifier macromodels requires understanding their limitations

Page 69

PRECISE POWER MANAGEMENT.

IT TAKES THE PAIN OUT OF DESIGNING LOW-POWER ICs

Increasing feature, function and processing requirements make it harder than ever to manage power consumption in personal electronics, wireless and handheld devices. A design system that concurrently analyzes and optimizes your IC for power, timing, area, signal integrity and yield is what you need. And that's what Magma provides. Blast Power™ and Blast Rail™NX facilitate significant power reductions throughout the flow, enabling you to complete low-power chips faster. Your design will blow the socks off your competitors' chips but won't blow your power budget, or your schedule.

For more on how Magma lets you get the most out of your chips with just the right amount of power, visit **www.magma-da.com/4LowPower**. Find out why the world's top chip companies rely on Magma software to design their most critical ICs.

MAGMA®

WORLDWIDE SELECTION
PERSONALIZED SERVICE

Access to over **540,000** part numbers from more than **320** quality, name-brand manufacturers!

#1 for Breadth of Product

#1 for Availability of Product

#1 for On-Time Delivery

#1 for Overall Performance

Source: EE Times Distributor Evaluation Study, September 2005

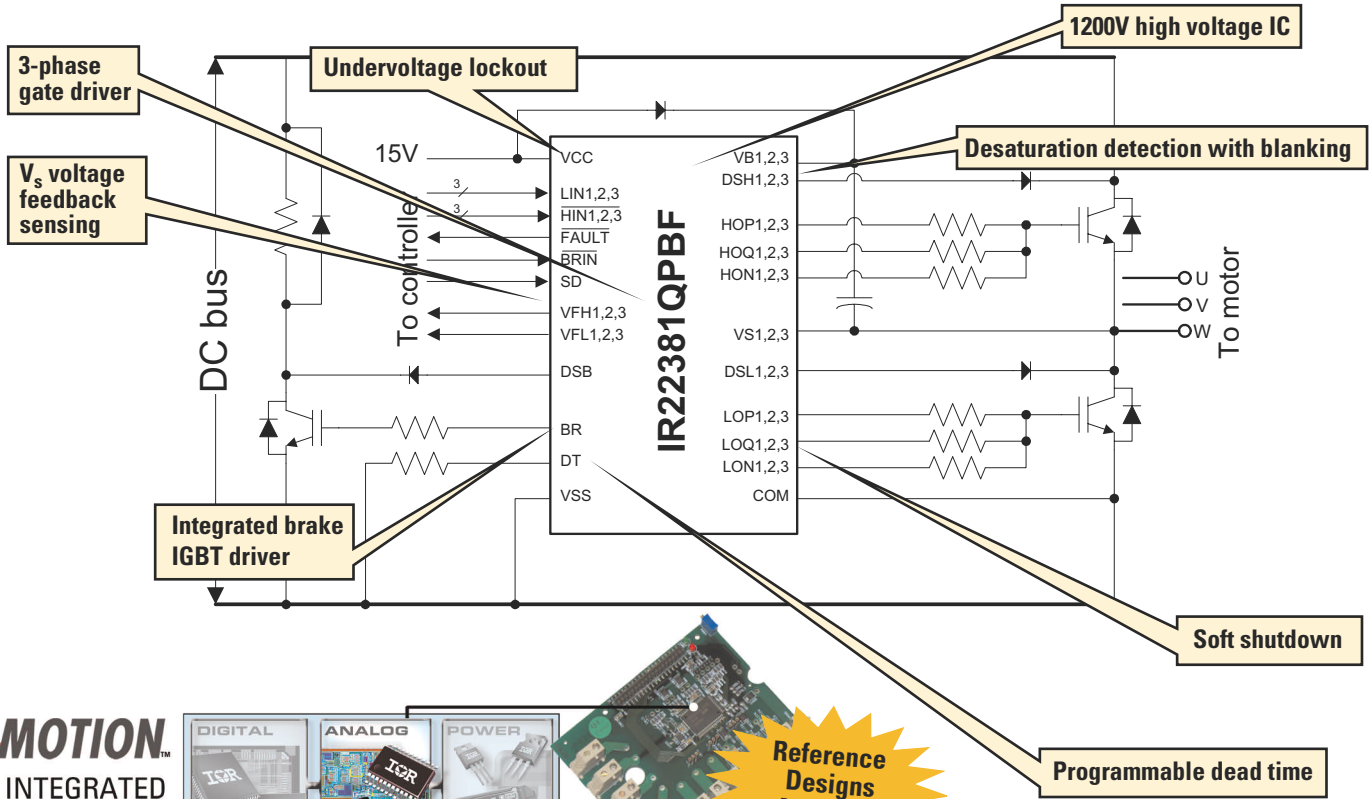
Digi-Key® CORPORATION

1.800.344.4539

www.digikey.com

RUGGED 1200V ICs DRIVE AND PROTECT YOUR MOTOR

High Voltage ICs Provide Dedicated, Reliable Industrial Solution



*i*MOTION™
INTEGRATED DESIGN PLATFORM

Reference Designs Available

Inverter Power	<3kW		>3kW	
Specifications	IR2233xPbF	IR22381QPbF	IR2213SPbF	IR22141S
Configuration	3-phase driver	3-phase driver	half-bridge driver	half-bridge driver
Voltage	1200V	1200V	1200V	1200V
Dead time (DT)	250ns	1µs	N/A	330ns
Soft shutdown duration time	No	6.0µs	No	9.25µs
t_{on}/t_{off}	750/700ns	550/550/ns	280/225ns	440/440ns
Matching delay	No	100ns	30ns	75ns
Drive Current $I_{o+}/_{o-}$	190mA/380mA	220mA/460mA	2.0A/2.5A	2.0A/3.0A
Desaturation blanking time	No	4.5µs	No	3µs
Independent half-bridge driver	Yes	No	Yes	No
Undervoltage lockout	Yes	Yes	Yes	Yes
Integrated brake driver	No	Yes	No	No

*i*MOTION is a trademark of International Rectifier.

FEATURES

- High and low side gate driver IC
- Integrates low voltage driver with high voltage level shifter
- IR industry leading, high voltage technology
- Single, rugged, compact IC

IR's *i*MOTION brings digital controllers, analog stage and power modules together in one easy to implement, integrated design platform.

for more information call 1.800.981.8699 or visit us at
www.irf.com/motion

International
IOR Rectifier
THE POWER MANAGEMENT LEADER

Don't let poor performance spoil your designs. With high performance AVR® microcontrollers you can create applications with no worries about the microcontrollers performance. AVR Flash microcontrollers operate with clock rates up to 20 MHz, achieving close to 20 MIPS. With 32 general purpose registers, the AVR delivers unmatched performance and flexibility while reducing power consumption to a minimum.

Learn more and try to unmask the Super AVR at www.atmel.com/ad/superAVR

ATMEL®

Everywhere You Are®

NI TestStand – The Industry Standard in Test Management Software

NI TestStand is a ready-to-run test management environment from National Instruments for automating your test and validation systems. With NI TestStand you can:

- Develop, manage, and automate your test sequences
- Simplify your maintenance through a modular, fully customizable test-system framework
- Leverage toolkits and add-ons from NI TestStand product and solution partners
- Execute test modules written in any programming language
- Specify sequence flow, reporting, database logging, and connectivity to enterprise systems
- Maximize test throughput with built-in parallel and batch execution and synchronization

To learn how Symtx and other electronic manufacturers are accelerating development and reducing costs, visit **ni.com/teststand**.

(800) 891-8841

NATIONAL INSTRUMENTS™

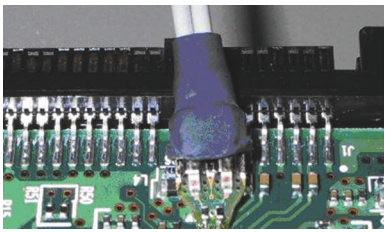
EDN VOICE OF THE ENGINEER 50 years

contents

5.11.06

Designers cast a skeptical eye on mixed-signal SOCs

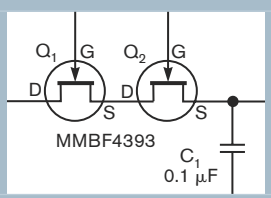
Hazardous-voltage primer



Spread-spectrum clocking: measuring accuracy and depth

Effective use of IC-amplifier macromodels requires understanding their limitations

DESIGNIDEAS



▶ Send your Design Ideas to EDNdesignideas@reedbusiness.com.

NEC ELECTRONICS AMERICA

A new army of 32-bit microcontrollers.

Introducing 28 additions to our V850 forces.

Flash:	V850 32-Bit All Flash Lineup								
640 KB					48 KB GC			48 KB GJ	
512 KB					40 KB GC		20 KB GJ	40 KB GJ	
384 KB					32 KB GC/GF		★20 KB GJ	32 KB GJ	
256 KB			12 KB GC	12 KB GK	16 KB GC/GF	12 KB GC	24 KB GC/GF	16 KB GJ	12 KB GJ	24 KB GJ
128 KB	4 KB GB	6 KB GB	6 KB GC	12 KB GK	6 KB GC/GF	12 KB GC	12 KB GC/GF	6 KB GJ	12 KB GJ	12 KB GJ
64 KB		6 KB GB		12 KB GK						
	Pin Count:	64		80			100			144

= V850ES/**Kx2** (2.7V to 5.5V operation)
= V850ES/**Hx2** (5V with up to 24 channels of 10-bit A/D)
= V850ES/**Jx2** (3V high performance)
KB = RAM Size ★ = 376 KB Flash Memory

GB= 10x10 mm **GK**= 12x12 mm **GC**= 14x14 mm **GF**= 14x20 mm **GJ**= 20x20 mm

These V850™ flash microcontrollers are fully equipped to take on whatever your mission entails.

- High performance real-time microcontrollers with high throughput
- Low power consumption with flexible power management
- Exceptional EMI/EMS performance
- All flash product lineup with a wide range of memory sizes and packages

Put a V850 device in your next design. Learn more at www.am.necel.com/28mcus and get an evaluation kit for just $49 (limited time offer).

Empowered by Innovation NEC

contents 5.11.06

pulse

Dilbert 24

DEPARTMENTS & COLUMNS

PRODUCT ROUNDUP

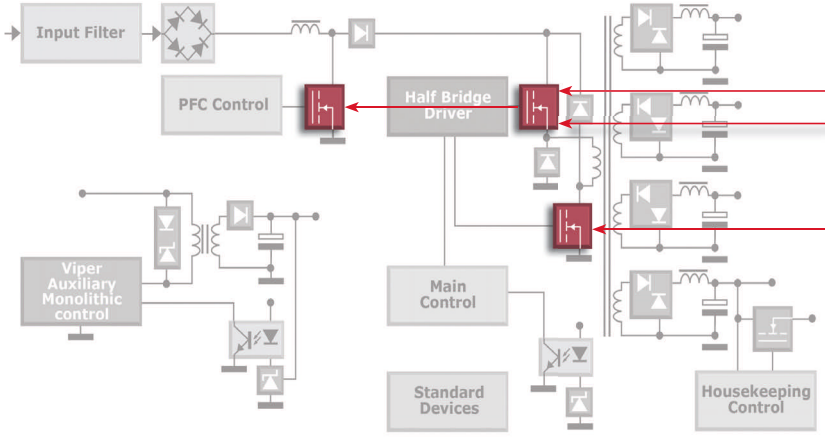
EDN® (ISSN#0012-7515), (GST#123397457, R.B.I. Intl Pub Mail #0280844) is published biweekly, 26 times per year, by Reed Business Information, 8878 Barrons Blvd, Highlands Ranch, CO 80129-2345. Reed Business Information, a division of Reed Elsevier Inc, is located at 360 Park Avenue South, New York, NY 10010. Tad Smith, Chief Executive Officer; Stephen Moylan, President, Boston Division. Periodicals postage paid at Littleton, CO 80126 and additional mailing offices. Circulation records are maintained at Reed Business Information, 8878 S Barrons Blvd, Highlands Ranch, CO 80129-2345. Telephone (303) 470-4445. POSTMASTER: Send address changes to EDN®, PO Box 7500, Highlands Ranch, CO 80163-7500. EDN® copyright 2006 by Reed Elsevier Inc. Rates for nonqualified subscriptions, including all issues: US, $165 one year; Canada, $226 one year, (includes 7% GST, GST#123397457); Mexico, $215 one year; air expedited, $398 one year. Except for special issues where price changes are indicated, single copies are available for $10 US and $15 foreign. Publications Mail Agreement No. 40685520. Return undeliverable Canadian addresses to: Deutsche Post, 4960-2 Walker Road, Windsor ON N9A 6J3. E-mail: subsmail@reedbusiness.com. Please address all subscription mail to EDN®, 8878 S Barrons Blvd, Highlands Ranch, CO 80129-2345. EDN® is a registered trademark of Reed Elsevier Properties Inc, used under license. A Reed Business Information Publication/Volume 51, Number 10 (Printed in USA).

Power Supply & Management

Solutions

MDmeshII Power MOSFETs with super-low $R_{DS(on)}$ give even lower power losses and easier driving for all your high-frequency SMPS applications.

Innovative products for multi-segment application systems



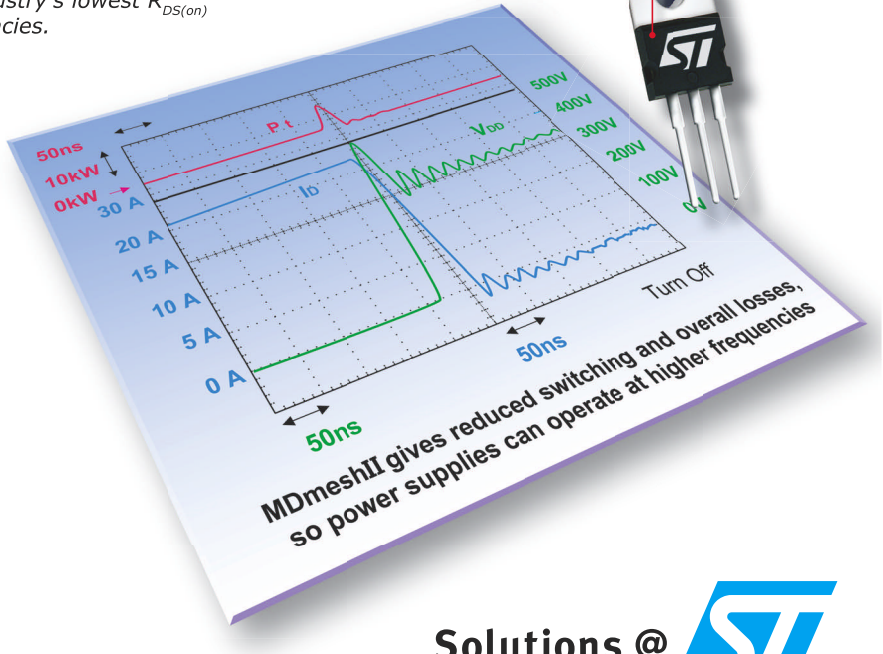
With ST's global solutions offerings such as Power Management ICs, Switching and Low Drop Regulator ICs and a wide range of advanced discrete devices, designing an SMPS for your application is easier than ever. The STP25NM60N using ST's unique MDmeshII™ technology, for example, offers one of the industry's lowest $R_{DS(on)}$ and new levels of performance at high frequencies.

Key Features

- Up to 40% on-resistance reduction
- Typical $R_{DS(on)}$ = 0.140Ω
- High dv/dt and avalanche capabilities
- 100% avalance tested
- Low input capacitance and gate charge
- Low gate input resistance

Part Number	V_{DSS} (@Tjmax)	$R_{DS(on)}$	I_D	Pkge.
STB25NM60N-1	650V	< 0.170Ω	20A	I²PAK
STF25NM60N	650V	< 0.170Ω	20A*	TO-220FP
STP25NM60N	650V	< 0.170Ω	20A	TO-220
STW25NM60N	650V	< 0.170Ω	20A	TO-247
STB25NM60N	650V	< 0.170Ω	20A	D²PAK

* Limited only by maximum temperature allowed



For datasheets, application notes and more information visit
www.st.com/mdmesh

MDmeshII is a trademark of STMicroelectronics.

Solutions @

DEVICE AVAILABLE FROM THESE DISTRIBUTORS: ARROW • AVNET • DIGI-KEY • FUTURE • MOUSER • NU-HORIZONS

EDN online contents

www.edn.com

ONLINE ONLY

Check out these online-exclusive articles.

ZigBee chip project offers SOC challenges

Design decisions: Geographically dispersed engineering team takes on integration of internal and third-party IP for RF SOC.

→www.edn.com/article/CA6325290

USB-hub chip accepts hospitality of two hosts

The device enables a single USB hub to furnish not one but two host systems with access to a set of attached peripherals.

→www.edn.com/article/CA6325520

Good engineers are worriers

The 2006 Electronic Design Processes Workshop did an admirable job of putting many of the industry's worries on the table.

→www.edn.com/article/CA6326107

Offerings advance audio at home, on the road

New additions to the toolbox include DSPs for low-cost home and automotive systems and a certified design for home-based HD Radio receivers.

→www.edn.com/article/CA6324252

Guest opinion: Will the real ESL please stand up?

The industry is still waiting for a truly disruptive technology to become the universally acknowledged design methodology.

→www.edn.com/article/CA6326108

READERS' CHOICE

A selection of recent articles receiving high traffic on www.edn.com.

Tackle noise from three perspectives

You've got noise in your circuit? Where do you look to find it?

→www.edn.com/article/CA6321523

Design Idea: Shift registers and resistors deliver multiphase sine waves

This simple method uses only digital logic and fixed-value resistors.

→www.edn.com/article/CA6321527

Design Idea: Use a switching-regulator controller to generate fast pulses

Switching-regulator-controller ICs can deliver gate-drive pulses with rise and fall times of less than 2 nsec, making them ideal candidates for laboratory pulse generators.

→www.edn.com/article/CA6321526

End of memory relationship may impact handsets

M-Systems and Samsung's parting of ways may have huge implications for high-end cell phones.

→www.edn.com/article/CA6324003

Design Idea: Isolated-FET pulse driver reduces size, power consumption

Drive a capacitive-input power device with any duty cycle at frequencies to 200 kHz.

→www.edn.com/article/CA6317069

***EDN*'s 2006 Digital Signal Processing Directory**

→www.edn.com/dspdirectory

Check out Technical Editor Robert Cravotta's annual directory of DSP devices and cores—an easy-to-browse yet exhaustive resource that features:

- Robert's incisive summary of every product family from every vendor
- Tons of downloadable PDF tables that allow you to zoom in on the DSP resources you need for your design
- Downloadable architectural block diagrams
- A sidebar ("Where did they go?") that helps you track where certain DSP offerings have ended up by virtue of acquisitions and other vendor moves.

FROM THE VAULT

Items from the EDN *archives that relate to this issue's contents.*

DESIGNERS CAST A SKEPTICAL EYE ON MIXED-SIGNAL SOCs (pg 48):

Enabling analog-IP reuse: relating requirements to reality

→www.edn.com/article/CA409045

HAZARDOUS-VOLTAGE PRIMER (pg 39):

Circuit-protection methods yield more robust products (includes some explosive video clips)

→www.edn.com/article/CA514947

Safety isolation protects users and electronic instruments

→www.edn.com/article/CA454635

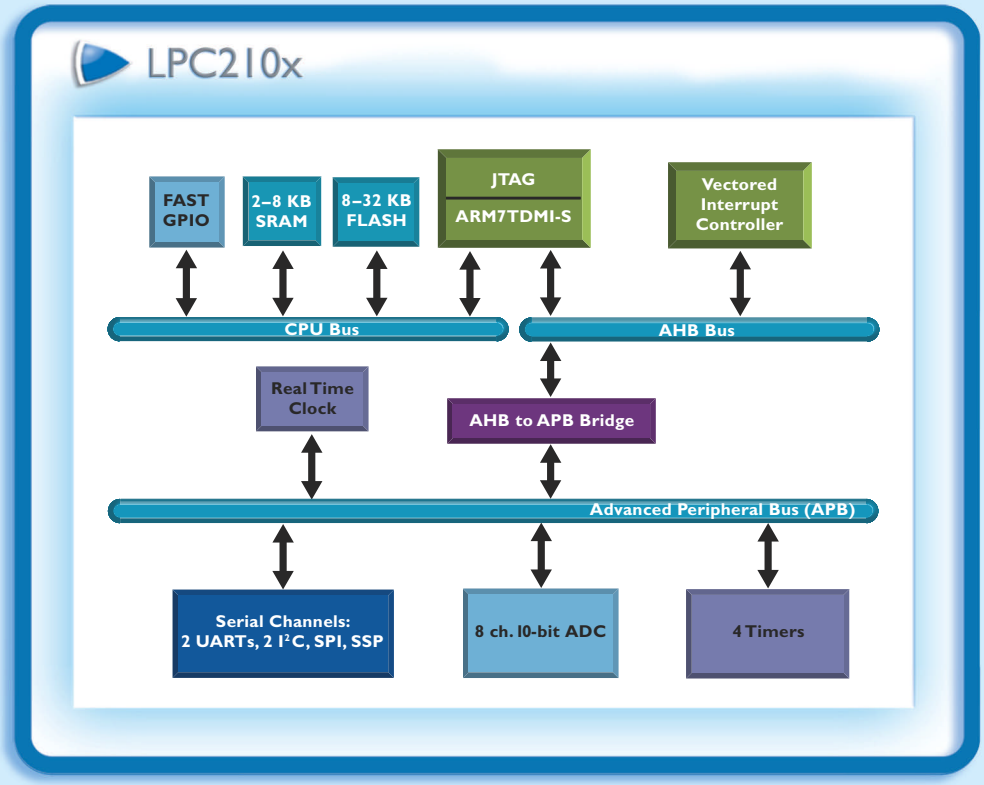
SPREAD-SPECTRUM CLOCKING: MEASURING ACCURACY AND DEPTH (pg 61):

Engineers still suffering from jitter jitters

→www.edn.com/article/CA6305400

12.5-Gbps serial BERT characterizes jitter

→www.edn.com/article/CA6279640



High-Performance Low-Cost Solution.

32-bit Flash Microcontrollers. The Philips LPC210x ARM7TDMI-S™-based MCU can help you with your application challenges by providing you with the industry's fastest ARM7-based microcontroller.

An easy upgrade path, minimal relearning

Single-chip solution with lots of peripherals

- On-chip Flash
- Timers, PWM, UARTs, SPI/SSP, I²C
- ADC
- Predictable, deterministic performance
- No cache required
- Same performance between Flash and RAM code execution

Low power for battery-operated applications

- <10uA power down, <1 mW/MHz active

Fast I/Os to implement interfaces, handshaking functions in software

High-performance 32-bit solutions at 8-bit MCU pricing

Highly reliable Flash memory

Low-cost tools support

For more information, please visit www.philips.com/microcontrollers

PHILIPS
sense and simplicity

Arrow AVNET electronics marketing FUTURE ELECTRONICS Digi-Key CORPORATION

Support **Across The Board.**™

Starting with in-depth design support all the way through to total supply chain management – Avnet Electronics Marketing is there for you. From concept to reality, we deliver:

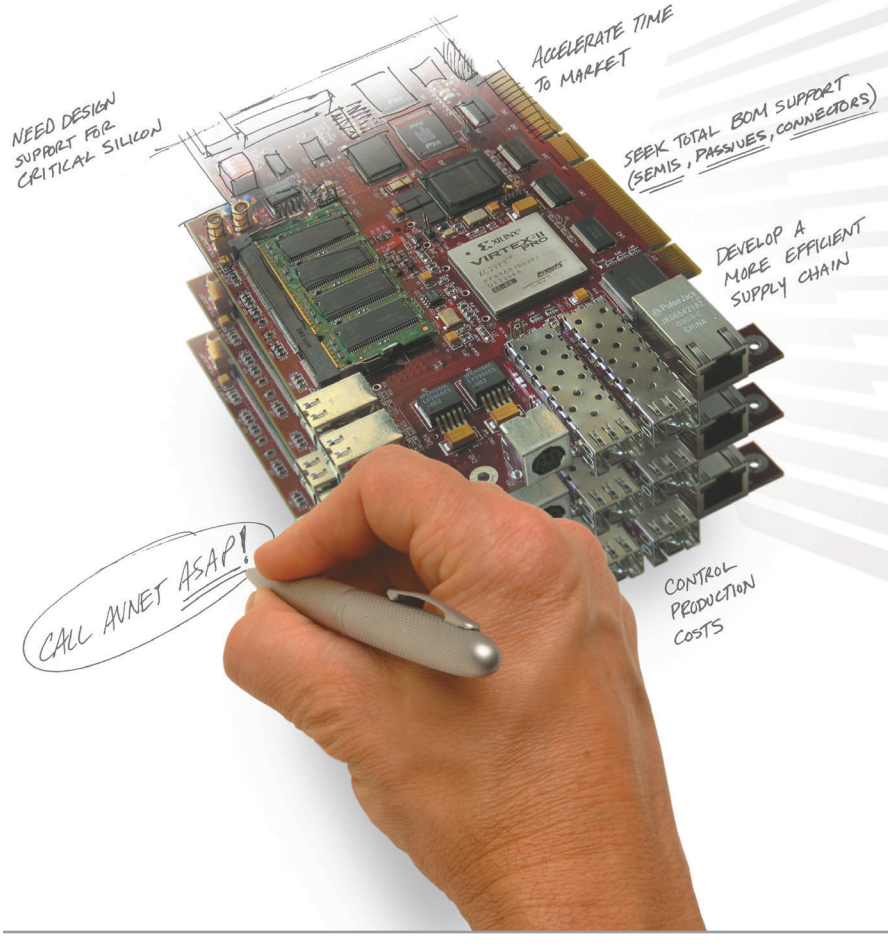
Consultative engineering support and services

Focused product specialization

The broadest supplier partnerships in the industry

Over $1 billion in top moving inventory "on the shelf"

World-class supply chain services



But, partnering with Avnet Electronics Marketing means much more than just having access to the industry's broadest array of design and supply chain services. It means working with a company that is truly focused on exceeding your needs and expectations – a company that is dedicated to giving you **Support Across The Board.**™

Ready.
Set.
Go to market.™

AVNET® electronics marketing

Enabling success from the center of technology™

1 800 332 8638
www.em.avnet.com

Avnet Green Initiative

NEDA Supplier Authorized Distributor

BY MAURY WRIGHT, EDITOR IN CHIEF

Mind of the engineer

I recently wrote about our commitment to serving the reader and, briefly, our belief in perpetual research to measure our performance and to understand our readers (**Reference 1**). In this issue, I share some recent research with you. Every two years, we do a major study, "Mind of the Engineer." The early results are back from the latest incarnation.

This year, we fielded the study worldwide and have statistically valid results from North America, Europe, China, Japan, and other parts of Asia. Almost 50% of the respondents are design-and-development engineers, and most of the rest split between pure R&D and engineering management. The results that I present here are specific to North America except where noted.

Let's start with what you indicate to be your greatest challenges today. Number one on the list is keeping up with the latest technologies. Other top mentions include shorter design cycles, outsourcing/offshore concerns, and working with fewer resources. Here's one direct response: "It is a must to keep current with the world, even if it does not directly affect me at this time." I suppose none of the responses is a surprise. You can perhaps take solace in knowing that you don't face them alone.

We asked how many projects you work on over the course of a year. Nine is the average, although those of you working in the consumer and computer segments reported 10 and 11, respectively. Numbers from other regions are generally lower; engineers in China work on only five projects per year. In North America, the automotive segment stands out; those working in that segment report that they work on 17 projects a year. I'd like to better understand that number. Perhaps it's due to the fact that engineers in the automotive segment have more overlapping long-term projects. Generally, almost all respondents report working on more projects now than in the past.

Clearly, you face pressure to excel in multiple design disciplines, with 58% reporting an increase over the past two years.

The study also reveals an increase in the number of you that work in teams—a trend that continues from past Mind of the Engineer studies. Today, 48% report working on teams, although the figure zooms to 62% for engineers under the age of 39.

For those of you actively working in teams, 31% have team members outside North America. More of those team members are in Western Europe than elsewhere, but 36% report working with team members in China, 26% in India, 19% in Taiwan, and 12% in Japan.

We also asked about how you divide your time at work and what increased responsibilities you have assumed. Clearly, you face pressure to excel in multiple design disciplines, with 58% reporting an increase over the past two years. With thin resources, analog specialists must be able to handle some digital work. We've found that FPGA designs have become the province of software specialists. I don't expect the trend to end.

Most of you—81%—also now support your designs through manufacturing. That number is fairly consistent worldwide with the exception of Japan, where only 39% of respondents support their designs through manufacturing. One North American engineer states, "The greatest challenge for me has been to deal with the expanding scope of the design-engineering process. Besides the basic engineering functions, I have had to become knowledgeable in all phases—from initial concept to manufacturing."

You also have to tolerate the fragility of the product-development process. On average, only 59% of your projects reach the market. The number of canceled projects soared in the 2000-to-2002 time frame, but I am frankly surprised that the success rate isn't higher today. The numbers are fairly consistent across application segments, as well. And only Europe stands out globally with only 45% of projects making it to market.

I'd like to thank all of you who participated in the study. We truly value your input. I welcome comments and questions. E-mail mgwright@edn.com, call 1-858-748-6785, or comment in the "Feedback Loop" in the online presentation of this column.

REFERENCE

1 Wright, Maury, "Serving you: the *EDN* mission," *EDN*, April 13, 2006, pg 14, www.edn.com/article/CA6321530.

If you're doing POL or VRM, check out our SLC, MVR, MLC or SER.

SLC7530	SLC7649	SLC1049	MVRT	MVRC	MLC1200	MLC1500	SER1360	SER1590	SER2000
0.05 - 0.4 µH	0.04 - 0.1 µH	0.08 - 0.15 µH	0.25 -0.56 µH	0.36 - 2.3 µH	0.36 - 4 µH	0.5 - 4.5 µH	0.33 - 10 µH	0.3 - 1 µH	0.3 - 2 µH
Up to 50 A	Up to 100 A	Up to 61 A	Up to 35 A	Up to 36 A	Up to 37 A	Up to 32 A	Up to 48 A	Up to 50 A	Up to 100 A
6.7 x 7.5 mm	7.5 x 7.6 mm	6.9 x 10.2 mm	9.8 x 11.5 mm	9.8 x 11.5 mm	10.5 x 11.2 mm	13.2 x 13.8 mm	13.1 x 12.9 mm	16.3 x 15.8 mm	19.6 x 20.1 mm
3 mm high	5 mm high	5 mm high	5.1 mm high	4.7- 7.8 mm high	4.1 - 6.1 mm high	3.9 - 6.5 mm high	5.8 mm high	10.2 mm high	8.6 - 14 mm high

And get samples PDQ.

Only Coilcraft offers such a broad range of high current, low DCR power inductors.

They're perfect for Point of Load and Voltage Regulator applications. Or any place you need maximum current handling in minimum space.

Several models are rated up to 100 A rms. Others have powdered iron cores for maximum saturation current and minimum thermal aging. Still others offer 5% DCR tolerance, making them ideal for current sensing applications.

As always, you can get free evaluation samples from our web site with just a click of the mouse. We ship same day!

Check out our full line of POL and VRM magnetics ASAP. Visit **www.coilcraft.com/POL3**

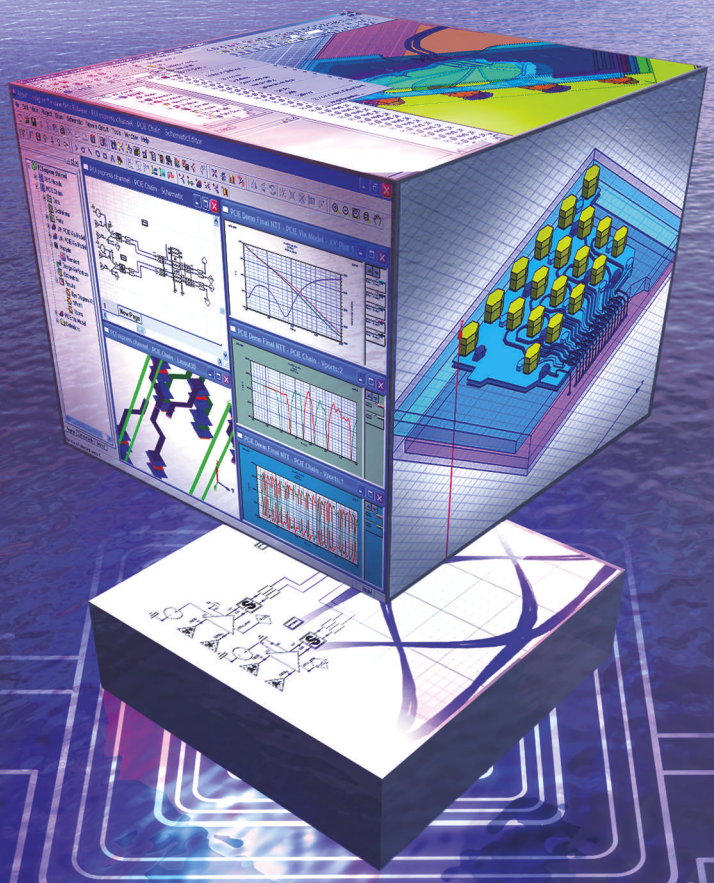
ORDER DIRECT
800-322-2645
OVERNIGHT DELIVERY! CALL BY 5 CST.

RoHS COMPLIANT

Coilcraft®

www.coilcraft.com 800/322-2645

HIGH-PERFORMANCE SIGNAL INTEGRITY SIMULATION SOFTWARE



NEXXIM®
Time and frequency-domain circuit simulation to predict multi-gigabit channel performance including S-parameters and transistor-level effects of drivers and receivers

HFSS™/Q3D EXTRACTOR®
GHz-accurate S-parameter and Full-Wave Spice™ models for complex trace routing, vias and transitions, connectors and IC packages

SIWAVE™
Full-board and full-package interconnect extraction for signal and power-integrity analysis

DESIGNERSI™
System-level signal integrity analysis with dynamic links to Nexxim and HFSS

ANSOFT

ANSOFT.COM

FRAM memory for high-speed data collection

FM20L08 - 1-Megabit FRAM Memory

- SRAM compatible - JEDEC 128Kx8 SRAM pinout
- 60ns access time & unlimited read/write endurance
- True nonvolatile RAM - no battery required
- Low power - 3-volt operation
- Significant board space savings - 32 pin TSOP

FRAM memory is optimized for nonvolatile data storage in a wide variety of applications. FRAM writes as fast as it reads, it's nonvolatile, and offers virtually unlimited write cycles. No algorithms or protocols are needed to write data and FRAM is byte addressable like SRAM.

System designers are putting the advantages of FRAM to work in a broad range of system applications from industrial equipment to plasma and LCD televisions. FRAM memories are also collecting data for world's largest digital utility meter installation and are storing data in some of the finest automobiles.

Find out how FRAM memory can raise the standard in your next design by calling a Ramtron technical engineer at 1-800-545-3726 or simply e-mail framinfo@ramtron.com

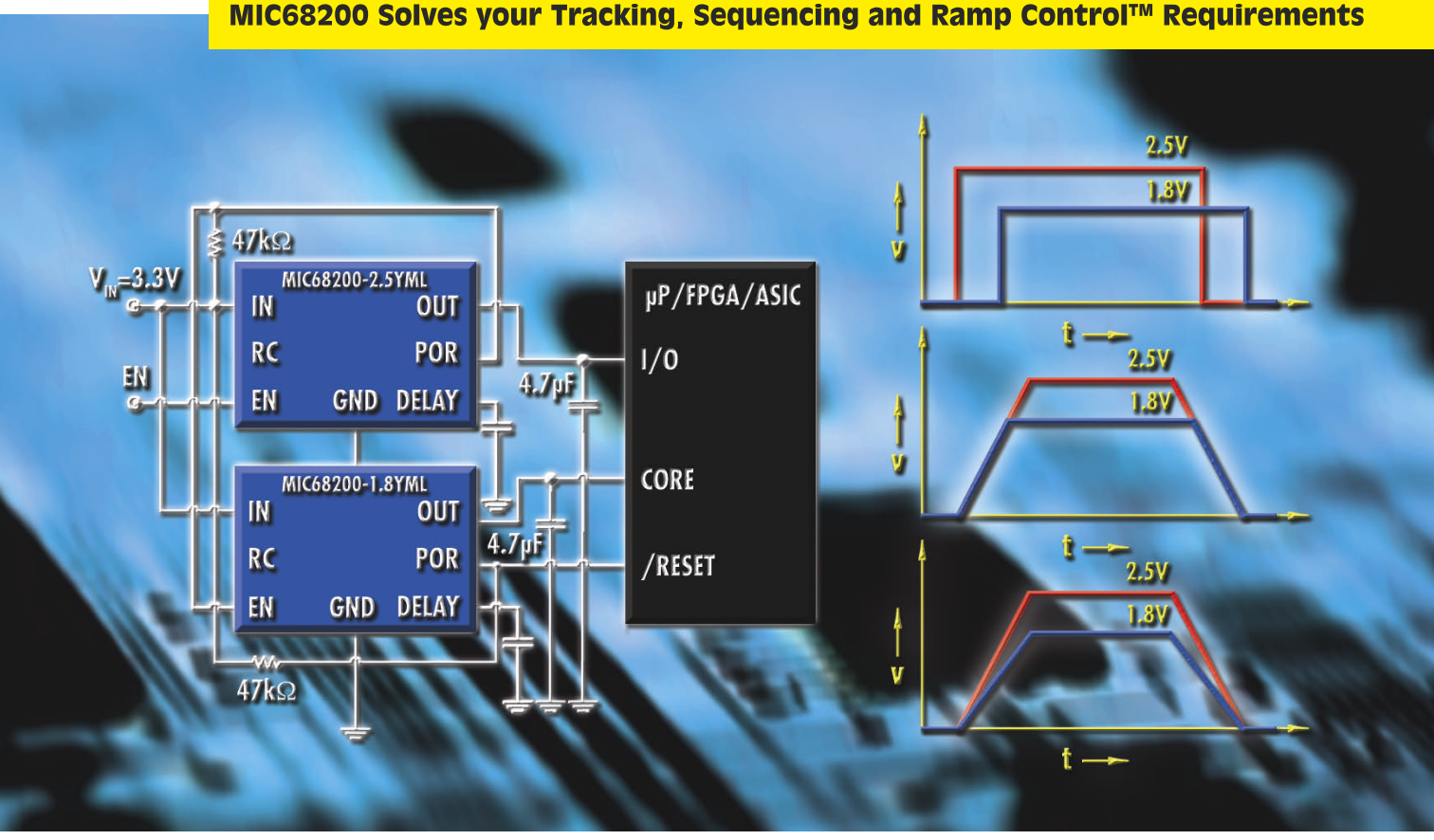
Download a Free FRAM Short Form Catalog today at www.ramtron.com.

www.ramtron.com

RAMTRON
International Corporation

Get on Track with Micrel Sequencing

MIC68200 Solves your Tracking, Sequencing and Ramp Control™ Requirements



ASIC, FPGA and CPU manufacturers require complex and unique start-up protocols for loads on the system board. Micrel's MIC68200 is designed specifically to address those protocols and make the task of the system designer simpler.

The MIC68200 operates from a wide input range of 1.65V to 5.5V, which includes all of the main supply voltages commonly available today. It is designed to drive digital circuits requiring low voltage at high currents. The chip incorporates a delay pin (Delay) for control of power on reset output (POR) at turn-on and power-down delay at turn-off.

Additionally, there is a ramp control pin (RC) for either tracking applications or output voltage slew rate adjustment at turn-on and turn-off. This is an important feature in applications where the load is highly capacitive and in-rush currents can cause supply voltages to fail and microprocessors or other complex logic chips to hang up. All power-up protocols, sequencing, window sequencing, tracking and ratiometric tracking can be implemented with minimal components, thereby eliminating the need for complex power management ICs.

For more information, contact your local Micrel sales representative or visit Micrel at: www.micrel.com/ad/mic68200.
Literature 1 (408) 435-2452 Information 1 (408) 944-0800

The Good Stuff:

- Input voltage range: 1.65V to 5.5V
- Stable with 4.7µF ceramic capacitor
- 1.0% initial output tolerance
- 2A maximum output current – peak start up
- 1A Continuous Operating Current
- Power-on Reset (POR) supervisor with programmable delay time
- Programmable Ramp Control for in-rush current limiting and slew rate control of the output voltage
- Tracking on turn-on and turn-off with pin strapping
- Timing Controlled Sequencing On/Off
- Single Master can control multiple Slave regulators

MICREL®

Innovation Through Technology™

www.micrel.com

ANALOG edge℠
Expert tips, tricks, and techniques for analog designs
Vol. IV, Issue 5
DESIGN idea

Overcoming Impedance Discontinuities in High-Speed Signal Paths by Using LVDS

by Brian Stearns, Principal Engineer

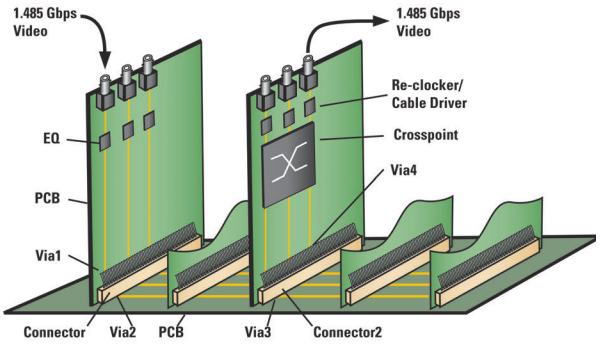


Figure 1. HD Video Router Diagram

At data rates from 400 Mbps to 1.5 Gbps, data signal paths become transmission lines. At these speeds the signal path model must include the reactive parasitic components in the cable or backplane. It is not just the data rate itself—the fast edge rates contain even higher frequency energy that react worse in distributed impedance environments. Ignoring parasitic impedances and impedance discontinuities above 200 Mbps will cause added noise in the transmission line, and data bit errors will occur.

Consider a basic High-Definition (HD) digital video router as an example of this challenge: HD video routers manage multiple HD source streams for distribution in broadcast, studio, or production video facilities. HD video channels operate from 270 Mbps up to 1.485 Gbps, demanding careful layout and consistent design practices to ensure the switching router system does not degrade the integrity of the video data.

In this system (***Figure 1***), an Adaptive Equalizer (EQ) receives the HD signal directly from the BNC connector. A common backplane connects the signals from the input card to the switch card for output to the desired destination channel. The signals travel point-to-point from the EQ across the PCB approximately 8 inches to the backplane connector, then across ~3 to 15 inches of backplane (depending on the slot used) to a second connector, then across another 8 inches of PCB to the inputs of the crosspoint switch device. A re-clocker/cable driver connects directly to the outputs of the crosspoint switch to drive the signals across cables. These HD video router systems are modular and may have anywhere from 8 to 1000 input/output channels. Therefore, signal density can be very high.

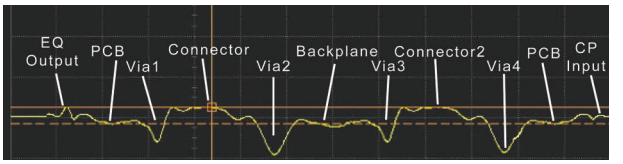


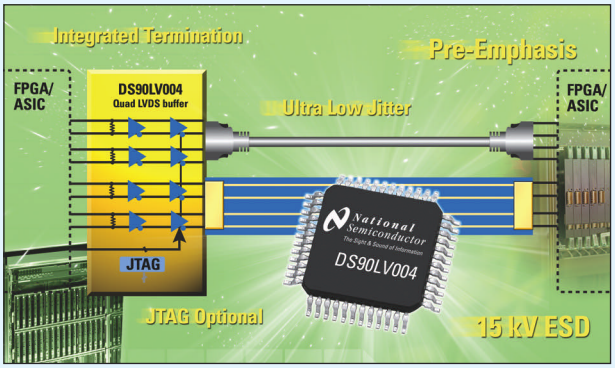
Figure 2. Example TDR Plot of Impedance Across the Signal Path (See *Figure 1* for discontinuity locations)

The common FR4 circuit board materials are a consistent impedance environment, but the distributed parasitic impedances will have a negative effect on the signal quality. Most affected are the fast edge rates as a result of the numerous frequency components operating higher than the fundamental data rate, causing signal losses and sluggish transition times. In addition, all the interconnections between the components (such as the BNC connectors, integrated circuits, vias between board layers, or the connectors between boards) can cause impedance mismatches from the characteristic impedance (Z_0), which will also affect signal quality (***Figure 2***). The dense backplane connectors inductively load the signal path,

NEXT ISSUE:
Voltage-Controlled Filter

National Semiconductor
The Sight & Sound of Information

Featured Products



Four-Channel LVDS Repeater with Pre-Emphasis

The DS90LV004 is a four channel 1.5 Gbps LVDS buffer/repeater. High-speed data paths and flow-through pinout minimize internal device jitter and simplify board layout, while configurable pre-emphasis overcomes ISI jitter effects from lossy backplanes and cables. The differential inputs interface to LVDS, and Bus LVDS signals such as those on National's 10-, 16-, and 18- bit Bus LVDS SerDes, as well as CML and LVPECL. The differential inputs and outputs are internally terminated with a 100Ω resistor to improve performance and minimize board space. The repeater function is especially useful for boosting signals for longer distance transmission over lossy cables and backplanes.

Features

- Hot-plug protection
- LVDS/CML/LVPECL compatible input, LVDS output
- On-chip 100Ω input and output termination
- 15 kV ESD protection on LVDS inputs and outputs
- Single 3.3V supply
- Very low power consumption

The DS90LV004 operates over a wide temperature range (-40 to +85°C) making it ideal for telecom, datacom, industrial, medical, automotive, and office imaging applications applications. It is available in a TQFP-48 package.

For FREE samples, datasheets, and more, visit
www.national.com/pf/DS/DS90LV004

Dual 1.5 Gbps 2:1/1:2 LVDS Mux/Buffer with Pre-Emphasis

The DS15MB200 is a dual-port 2 to 1 multiplexer and 1 to 2 repeater/buffer. High-speed data paths and flow-through pinout minimize internal device jitter and simplify board layout, while pre-emphasis overcomes ISI jitter effects from lossy backplanes and cables. The differential inputs and outputs interface to LVDS or Bus LVDS signals such as those on National's 10-, 16-, and 18- bit Bus LVDS SerDes, or to CML or LVPECL signals

Features

- 1.5 Gbps data rate per channel
- Configurable off/on pre-emphasis drives lossy back planes and cables
- Low output skew and jitter
- On-chip 100Ω input and output termination
- 15 kV ESD protection on LVDS inputs/outputs
- Hot-plug protection

The DS15MB200 features a 3.3V supply, CMOS process, and robust I/O ensure high performance at low power over a wide temperature range (-40 to +85°C) making it ideal for base-stations, DSLAMs, routers, switchers, and industrial systems applications. It is available in LLP-48 packaging.

For FREE samples, datasheets, and more, visit
www.national.com/pf/DS/DS15MB200

Overcoming Impedance Discontinuities in High-Speed Signal Paths by Using LVDS

while vias in the PCB capacitively load the signal path. Signal reflections will occur at any location along a transmission path where a change in impedance exists. These reflections and parasitic impedances will cause loss of signal amplitude, ringing, rise time degradation, and EMI.

In this example system there can be up to 31 inches of FR4 from the EQ outputs to the input of the crosspoint switch, with several impedance discontinuities along the way. If the speed of the incident edge is 175 to 200 ps/inch down this path, and the data rate is 1.485 Gbps (half-wavelength = 343 ps), then there can be as many as 18 transitional edges on the path at any given time. Reflections caused by the incident edge at impedance mismatches will affect all the edges present on the signal path. Reflections from edges 1 through 17 will greatly distort edge number 18 by the time it arrives at the end of the signal path. The resulting eye pattern (***Figure 3***) shows the loss of amplitude, excessive jitter, and rise/fall time degradation.

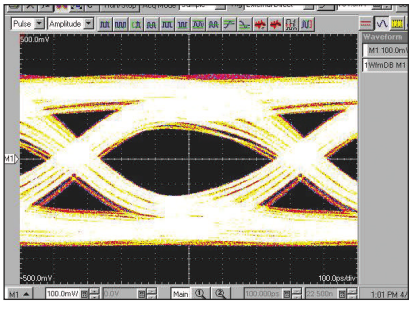


Figure 3. Eye Pattern at Input to Crosspoint Switch After 31" of FR4

One possible solution to this challenge is to use higher quality connectors between the daughter cards and the backplane. This will minimize the discontinuities of the connectors. Better via design will further flatten the TDR measurement plots so that the apparent impedance over the length of the signal path stays much closer to Z_0.

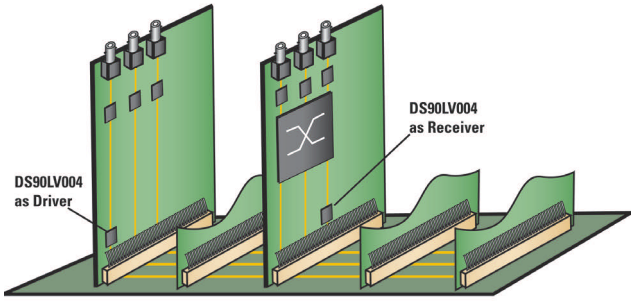


Figure 4. Buffer Locations to Overcome Impedance Discontinuities

Another, more cost-effective solution is to use a simple LVDS buffer, such as the DS90LV004, to drive and receive the signal across the backplane. This effectively breaks the transmission path into smaller segments to mask the impedance mismatch and diminish signal attenuation. Place a buffer at the edge of the daughter card to drive the connector and backplane, a second buffer on the switch daughter card to receive the signals (***Figure 4***), and re-drive them to the input of the crosspoint switch to effectively hide the impedance discontinuities between the two buffers (***Figure 5***). Proper terminations also ensure that the receiver absorbs all the energy in the line and none reflects back to the source.

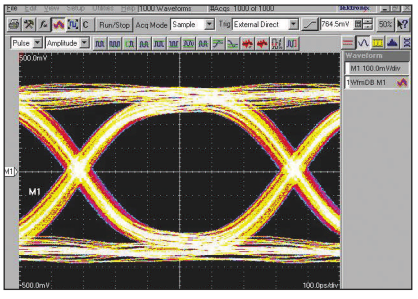


Figure 5. Eye Pattern at the Crosspoint Input with DS90LV004 Buffers Isolating the Backplane Connections

In addition, the buffers typically offer additional signal quality enhancements to improve the original signal. For example, buffers featuring input equalization will remove the deterministic jitter from the media losses before delivery across the backplane. Output pre-emphasis can boost the amplitude of the signal, further opening the eye pattern at the crosspoint inputs or receiver. High ESD ratings on the buffer I/O protect the other components on the daughter cards from ESD events elsewhere on the backplane.

Summary

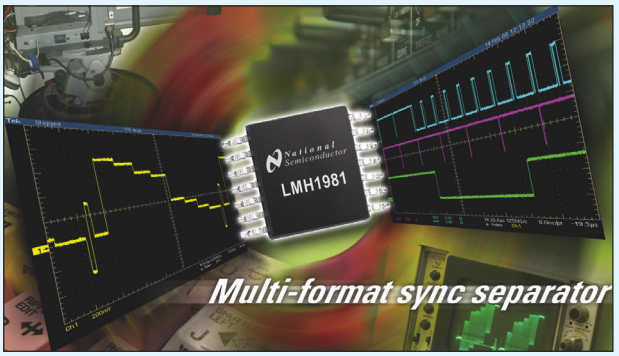
High-speed interfaces across backplanes require impedance control along the entire signal path. Using simple LVDS buffers to isolate impedance discontinuities or to shorten the interconnect lengths can reduce system costs and enhance the interface performance by eliminating the need for expensive high-frequency connectors. ■

Featured Products

Multi-Format Video Sync Separator

The LMH1981 is a multi-format sync separator for high-definition broadcast and professional video systems. The device automatically detects the input video format and performs all the necessary sync separation to generate low-jitter horizontal and vertical sync signals for standard and high-definition video formats, including NTSC, PAL, SECAM, 480i, 480p, 576i, 576p, 720p, 1080i, and 1080p.

The LMH1981 features the timing outputs needed for any video system, including horizontal, vertical and composite sync, odd/even field, burst/back porch clamp, and a patented automatic video-format detection feature. The device accepts both bi- and tri-level sync video inputs and features 50% slicing to ensure accurate separation of signals that vary in amplitude, offset, and noise. The device has a wide input range, allowing the inputs to accept video signals from 500 mV_{P-P} to 2 V_{P-P}.



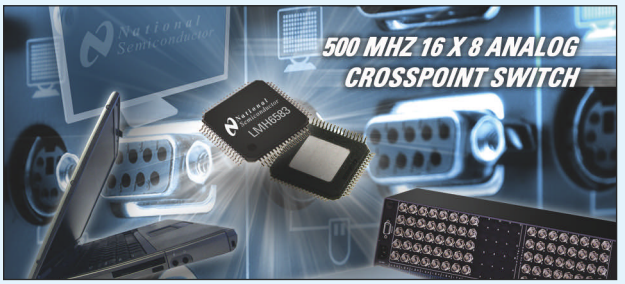
Features

- 50% Sync slicing
- Low jitter horizontal sync outputs
- Supports NTSC, PAL, SECAM, 480i, 480p, 576i, 576p, 720p, 1080i, and 1080p
- Accepts video signals from 500 mV_{P-P} to 2 V_{P-P}
- No external programming with µC required
- Horizontal sync output propagation delay <50 ns

The LMH1981 is ideal for use in a wide range of video applications such as, broadcast video equipment, video distribution, DTV and HDTV systems, and is available in TSSOP-14 packaging.

For FREE samples, datasheets, and more, visit
www.national.com/pf/LM/LMH1981.html

Analog Crosspoint Switches for High-Resolution Video Applications



The LMH® family of high speed amplifiers is joined by the LMH6582 and LMH6583 16 x 8 analog crosspoint switches. The devices are available in a gain of 1 (LMH6582) and gain of 2 (LMH6583) options and are completely non-blocking. Allowing an output to be connected to any input, including an input that is already selected. The devices can be used in distribution applications where each output is connected to the same input, also known as broadcast mode. The inputs and outputs are also fully-buffered, allowing impedance matching to any source at the inputs and capability to drive up to two back terminated 75Ω video loads on the outputs.

Designed on National's proprietary VIP10 process, both devices offer significant speed and crosstalk performance over competitive solutions. The 500 MHz of bandwidth and 0.1 dB gain flatness out to 100 MHz support high resolution video formats to QXGA (2048 x 1536) and beyond.

Features

- 500 MHz, -3 dB Bandwidth
- Fast slew rate: 3000 V/µs
- 100 MHz, 0.1 dB gain flatness
- Low crosstalk:
  - -70 dBc at 5 MHz
  - -50 dBc at 100 MHz
- Gain =1 and gain =2 options available
- Serial programming

The LMH6582 and LMH6583 are ideal for use in wideband routers and switchers, conference room systems, keyboard/video/mouse systems, multimedia video systems, and professional A/V systems. These products are available in a unique TQFP-64 package.

For FREE samples, datasheets, and more, visit
www.national.com/pf/LM/LMH6582.html
www.national.com/pf/LM/LMH6583.html

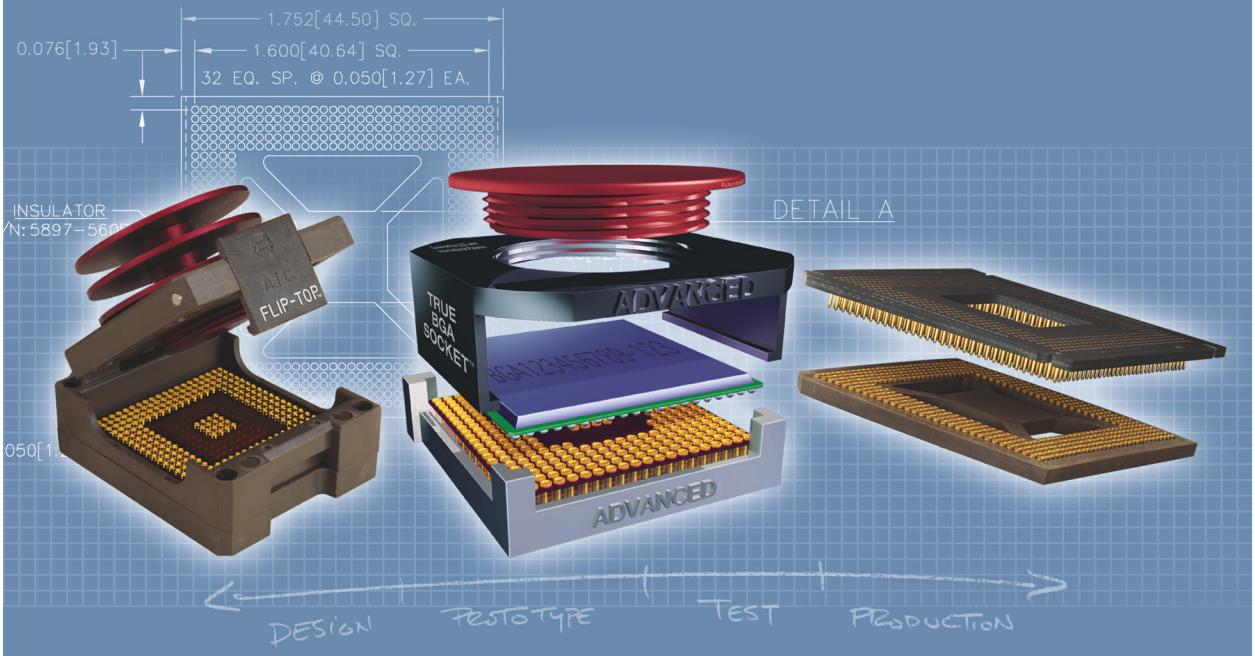
National Semiconductor
The Sight & Sound of Information

EDN
VOICE OF THE ENGINEER
50 years

EDN. 225 Wyman St, Waltham, MA 02451. **www.edn.com**. Phone 1-781-734-8000;
fax: 1-781-734-8070. **Address changes or subscription inquiries:** phone 1-800-446-6551; fax: 1-303-470-4280;
subsmail@reedbusiness.com. For a free subscription, go to **www.getfreemag.com/edn**. Reed Business Information, 8878
S Barrons Blvd, Highlands Ranch, CO 80129-2345. Include your mailing label.

Reed Electronics Group

We Create BGA Solutions From The Drawing Board To The PC Board.



And Every Step In Between.

Products shown may be covered by patents issued and/or pending.

Standard Eutectic or Optional Lead-free

Advanced now offers select BGA sockets with lead-free solder ball terminals to comply with worldwide directives.

From concept to completion, Advanced is your *single* source for comprehensive BGA socketing systems. We specialize in economical, dependable alternatives to direct device attach, with an array of innovative solutions for any stage of development. Whether you're using BGA, LGA or CSP devices in prototype or production applications — you can be sure we're with you every step of the way.

To learn more, visit us online at **http://www.bgasockets.com** or call **1.800.424.9850**.

ADVANCED INTERCONNECTIONS

5 Energy Way, West Warwick, Rhode Island 02893 USA

IC SOCKETS AND ADAPTERS ■ BOARD TO BOARD CONNECTORS ■ PEEL-A-WAY® CONNECTORS

ISO 9001

Fabless-ASIC company tries new model

Maybe the world isn't beating the bushes to find another fabless-ASIC company. But start-up Key ASIC believes that it has a model—an application-specific approach—that's just different enough to make a place for itself beside the relative giants, such as eSilicon (www.esilicon.com) and OpenSilicon (www.opensilicon.com). The company drew its digital engineers from hardware-optimization company Arcadia Design Systems (www.arcadiadesign.com) and its mixed-signal engineers from Intel (www.intel.com). Key ASIC now has two design teams comprising 30 engineers. Half of the members are in Silicon Valley, and half are in Malaysia. Working with a number of independent IP (intellectual-property) companies, the company has built up a portfolio that includes an ARM9 core, high-speed interface IP, audio and video—including HD—ADCs, and power-conversion blocks. The company targets the consumer and wireless-device markets.

The ARM9 illustrates the value added in Key ASIC's approach. Rather than simply pass a synthesizable core through to customers, the company uses customer specs to produce an optimized hard core with the speed, power, and cache configuration the customer needs. Presumably, the company will take a similar approach to the other critical datapaths in the customer's SOC (system-on-chip) design.

Key ASIC offers two-month turnaround on multidesign wafer-shuttle services, as well as full concept-to-production joint design with the customer. With its roots in Malaysia, the company has insider knowledge of the packaging, testing, and yield-engineering portions of the process. Key ASIC is currently offering 180- and 130-nm CMOS processes from Silterra (www.silterra.com) and TSMC (www.tsmc.com). Initial customer designs and some of the IP blocks are currently in shuttle runs, and the company expects to have production tape-outs this year.

—by Ron Wilson

▷**Key ASIC**, www.keyasic.com.

05.11.06

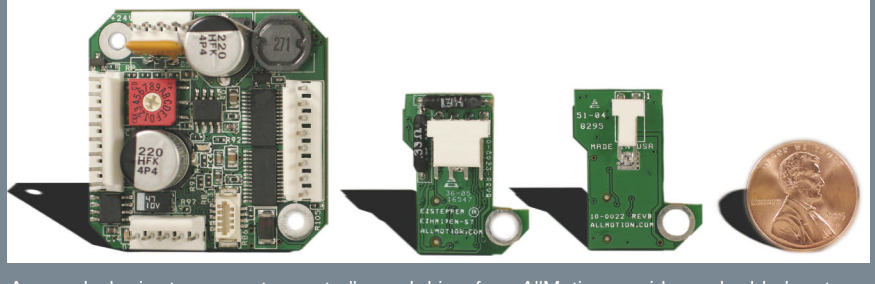
Compact controller eases embedded-system motion

Targeting medical devices, optical instruments, and embedded-system automation applications, AllMotion recently announced a dual-axis stepper-motor controller and driver. Measuring just 1.6×1.6 in., the EZHR17EN provides as much as 2A of drive current for one axis and as much as 1A for the second with an optional driver daughtercard. The EZHR17EN gives positioning, acceleration, and velocity capability to any stepper motor that is NEMA size 23 or smaller.

The EZHR17EN command set is compatible with devices using the Cavro DT or OEM medical-communications protocols, allowing high-speed, complex motion at speeds as high as 20 million microsteps/sec. Using the device, you can issue commands from any serial-terminal program, such as HyperTerminal, or from the EZ Stepper Windows application. With command strings and other programs in the onboard EEPROM, the EZHR17EN can operate stand-alone with no connection to a PC. A single four-wire bus can link as many as 16 stepper-motor controllers in a daisy chain. The EZHR17EN controller sells for $225, and the daughterboard costs $69.

—by Warren Webb

▶**AllMotion Inc**, www.allmotion.com.



A new, dual-axis stepper-motor controller and driver from AllMotion provides embedded-system designers with precision motion control in a compact package.

Software reduces cell-phone-test time by nearly an order of magnitude

According to Agilent Technologies, cellular-telecommunications-market analysts estimate that vendors this year will manufacture 800 million to 1 billion cell phones. Moreover, although many US customers never learn the exact price of their phones because US providers so often bundle the phone cost into the monthly charge for cellular service, the average customer's cost for a phone is rapidly heading lower—from perhaps $40 now to $20 or so within two years. Add to these statistics the phones' growing capabilities.

They now, for example, include built-in cameras, can play streaming audio and video, and can download large data files at high speeds. They can also operate in wider geographic areas, which implies the ability to operate in multiple frequency bands. All these features add up to a huge testing problem: Before shipping any handset, the manufacturer must prove that all of these capabilities work correctly.

In production test, time is money. Fortunately, the test community recognizes that cell-phone test hasn't made optimal use of the test time. Some current test protocols waste seven-eighths of the time. Several companies have developed ways to use this heretofore-wasted time. With the aid of new software, Agilent test equipment can increase the number of handsets it tests per unit of time by almost an order of magnitude. Agilent believes that it is the first company to offer such improvements. The company calls its 8960 the first one-box test set to perform production testing of phones that support the 1× EV-DO (evolution-data-optimized) Release A third-generation cellular-communication protocol and RF testing of such phones in R&D.

The 8960 one-box test set performs production testing of phones that support the 1× EV-DO Release A third-generation cellular-communication protocol and RF testing of such phones in R&D.

The term "1×" refers to one times the speed of TIA-EIA CDMA (code-division multiple access). The current speed of 1× EV-DO is approximately 2.4 Mbps downstream and 0.3 Mbps upstream. Over the next few years, these speeds and those of the competing HSPA (high-speed-packet-access) standard may increase by a factor of six.

Prices for the 8960 range from approximately $45,000 to $50,000, plus software. Including software, systems configured for production-test cost approximately $50,000 to $60,000, and those configured for R&D cost approximately $80,000 to $100,000.

—by Dan Strassberg

▷**Agilent Technologies**, www.agilent.com/find/8960, www.agilent.com/find/networkinabox.

FROM THE VAULT

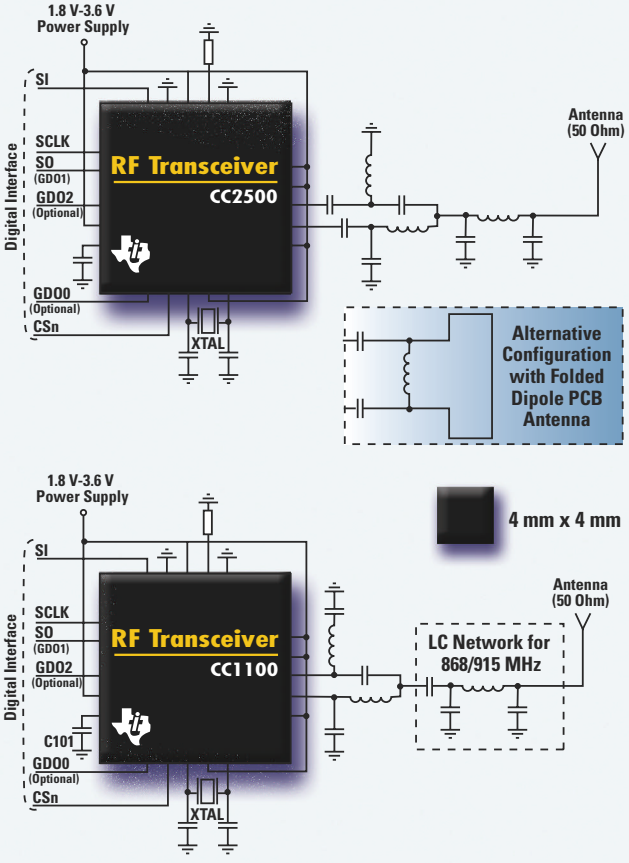
"Your future has been changed. The advent of the MOS/LSI chip-set microprocessors has catapulted you from lowly electron chaser to the heady heights of 'system architect.' You may not get any more money, but you'll be running some pretty big shows."

Robert H Cushman, former *EDN* special-features editor, Nov 5, 1973.

DILBERT *By Scott Adams*

2.4 GHz and Sub-1 GHz RF ICs

Ultra-Low-Power, Small Footprint, Lowest System Cost



The new **CC2500** and **CC1100** RF transceivers from Texas Instruments are the industry's lowest system cost, multi-channel radios for low-power wireless applications. Operating in the 2.4 GHz (CC2500) and sub-1 GHz (CC1100) frequency bands, the devices include several useful digital features like full packet handling, FIFO buffers, clear channel assessment, wake-on-radio and more.

Chipcon Products from Texas Instruments

▶ Applications

- Wireless game controllers
- Wireless keyboard/mouse
- Automatic meter reading
- Wireless audio
- Alarm and security systems
- Home and building automation

▶ Features

- Reference design with two-layer PCB with all components mounted on the same side
- Very small footprint: 4 x 4 mm, 20-pin QLP package
- Programmable data rate from 1.2 to 500 kbps
- Robust solutions with excellent selectivity and blocking performance
- Few external components
- Very low current consumption CC2500/CC1100:
  - T_X: 21.2/16.0 mA at 0 dBm
  - R_X: 13.3/15.2 mA at 250 kbps
- Pricing: $1.75 in 1K

NEW!
Low-Power RF Selection Guide
Datasheets and Samples

www.ti.com/cc2500-1100 ◦ 800.477.8924, ext. 2500

Technology for Innovators™

TEXAS INSTRUMENTS

DFM tools help with "lithography-friendly" layouts

Mentor Graphics claims that its latest DFM (design-for-manufacturing) offering will help IC designers make "lithography-friendly" IC layouts. The company's new Calibre LFD (lithography-friendly design) is similar to a DRC/LVS (design-rule-checking/low-voltage-signaling) tool. However, rather than check whether a layout conforms to design rules, such as trace widths and spacing, and early schematics, Calibre LFD checks whether a layout conforms to manufacturing-lithography rules that outline the dose and focus of a given manufacturing line. The tool incorporates the same engine as OPCVerify, a similar OPC (optical-proximity-correction) technology that Mentor introduced in January that targets lithography designers.

"Calibre LFD aims to capture process variation to improve design robustness," says Jean-Marie Brunet, product-development manager for LFD products at Mentor. The company has devised the Calibre LFD kit, an encrypted format that allows fab facilities to pass lithography information to layout engineers who are using Calibre LFD. The kit includes manufacturer-defined recipe information and process models with optical processes, resist masks, and, in some cases, etch profiles. After loading the kit into Calibre LFD, layout engineers feed the tool their design layouts. The tool then outputs a set of DRC-like markers, flagging rule violations, which users then have to fix with a separate layout tool. The tool reports different types of error from those that DRC tools do.

The tool also produces a DVI (design-variability index), which helps users identify topologies that are sensitive to variability. The DVI also ranks topology problems to help users make trade-offs when they adjust their layouts or even tweak design rules. A layout modification may have a positive impact on timing and yield, but it can create a problem for power. "For layout engineers to make an optimization, they need to have a reference point ... the ability to compare two layouts without requiring an in-depth understanding of lithography problems," says Brunet. Therefore, the tool assigns a DVI value to a given layout or even a piece of IP (intellectual property), and, the lower the DVI, the less susceptible the design is to variation across parameters.

Future releases of the tool will likely include features for fixing layouts. Mentor will maintain and update fab- and process-specific Calibre LFD kits as manufacturing processes at participating fabs evolve. The price for the tool starts at $246,000 for a one-year subscription.

—by Michael Santarini

▷**Mentor Graphics**, www.mentor.com.

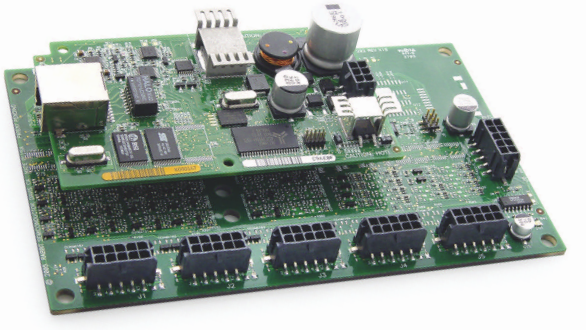
Process yields custom boards in five days

Hardware developers are constantly under fire due to the excessive leadtimes between the start of a new project and hardware availability. It often takes months to design, lay out, fabricate, and debug a custom embedded-processor board with a unique set of peripherals that exactly fits the project. At the Embedded Systems Conference last month in San Jose, CA, Rabbit Semiconductor addressed that problem by announcing the innovative RabbitFlex process for creating and manufacturing customized boards.

Customers can go to the Rabbit Web site and create designs by choosing from an array of available board options, including Ethernet, RS-232, RS-485, and RabbitNet, as well as analog- and digital-I/O circuits. All of these configurations reside in a customer-specific DesignID, which Rabbit then processes without NRE (nonrecurring-engineering) charges or setup fees. A streamlined manufacturing process results in the production of custom devices that the factory builds and ships within five working days.

RabbitFlex offers a base level single-board computer powered by either the 51.6-MHz PowerCore 3800 or the 25.8-MHz PowerCore 3810. In addition to serial and digital options, customers can select from as many as 16 ADC channels or two DAC channels. RabbitFlex also supports a matrix keypad and LCDs with or without backlighting. The vendor's Dynamic C software-development system supports RabbitFlex, and programming requires an interface cable from the PC to a RabbitFlex connector. The process creates a unique Dynamic C library for each RabbitFlex board whose design reaches completion. Once a customer purchases a board, the library becomes finalized. Prices for the RabbitFlex boards range from $149 to $279, depending on configuration. A RabbitFlex tool kit, supporting first-time development, sells for $199 and includes a development-software package, product documentation, programming cable, and accessories. An optional display/keypad-accessory kit is available for $69.**—by Warren Webb**

▷**Rabbit Semiconductor**, www.rabbitsemiconductor.com.



A new design-and-manufacturing process from Rabbit Semiconductor offers designers custom boards that the company automatically builds, tests, packages, and ships within five working days.

Turbo Charge Your Transient Response

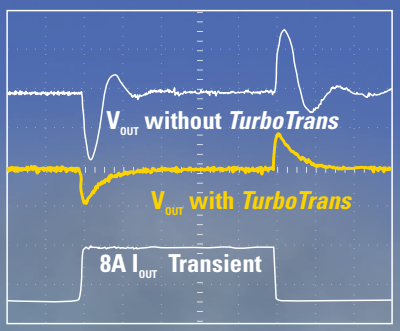
with new T2 Power Modules & *TurboTrans*™

Tired of adding capacitors to your power design? Introducing the T2 series – the second generation PTH modules with *TurboTrans*™ technology. This patented* technology provides up to an 8X reduction in required output capacitance while still meeting the stringent transient load requirements of DSPs, µPs, ASICs and FPGAs.

High Performance. Analog. Texas Instruments.

Order your sample now!
www.ti.com/T2

- *TurboTrans* technology
- 1.5% output regulation
- Up to 50% smaller footprint
- SmartSync synchronization
- Wide input voltage (4.5V to 14V)
- Auto-Track™ sequencing



Technology for Innovators™

Texas Instruments

VOICES

Chandu Visweswariah:

IBM innovation brings statistics to digital-IC design

Chandu Visweswariah, along with Kerim Kalafala, lead a team of R&D engineers at IBM Research and IBM Electronic Design Automation. Their small group recently won *EDN*'s Innovator of the Year award for developing the EinsTimer statistical-timing tool, which also took top honors in the EDA Design and Implementation Tools category. Their group also won the Design Automation Conference's best-technical-paper award in 2004, and the company commercially released the product before the Design Automation Conference in 2005.

What is statistical-timing analysis, and what problems does it tackle?

A Statistical-timing analysis traditionally handles process variations in a corner-based manner. In other words, the timer checks chip performance and timing relationships at various discrete "process corners." The main problems with this approach are that, in modern technologies, the number of corners can be large, and the technique does not lend itself to robust optimization. Statistical-timing analysis models gate and wire delays as probability distributions with complex correlations and predicts chip performance and parametric yield as probability distributions. The advantages of the new paradigm include fast turnaround, incremental operation for optimization, pessimism reduction, sensitivity prediction, and enablement of performance-versus-yield trade-offs.

Analog designers are used to statistical proofs, but why does the digital world need them?

A Digital designers relied on being able to bound their performance in a relatively straightforward way. But, now that wire delays play a larger role in determining performance and metal levels exhibit independent variations, it is no longer easy to bound performance. Because variability is a complex, multidimensional phenomenon, solid tool support is necessary to help circuit designers to maximize both parametric yield and performance.

Why will the technology become important in the future?

A As you move to 65-, 45-, and 32-nm processes, variability will only get worse. As you reach fundamental physical limits, you'll see the statistical nature of matter in dopant fluctuations,

oxide-grain boundaries, and line-edge roughness. Making individual worst-case scenarios of all these sources of variation will induce pessimism that will rob the new technologies of any performance gain. Besides, robust design and adaptive techniques will become more common. Hence, it is imperative that you embrace a statistical design-and-optimization methodology.

You said that launching the research program was difficult and required buy-in from management. What does management now think?

A Management is enthusiastic! Any new paradigm generates resistance and inertia, particularly if a delay or arrival time is no longer a number but a probability distribution instead! However, with the right combination of generating results, persistence, and perseverance, statistical techniques are finding their way into mainstream use, including in IBM's ASIC tool kit. IBM is introducing these techniques in a phased manner, and they are invaluable parts of accurate timing with reduced pessimism and fast turnaround. Better process modeling couples with statistical timing to be the best way to achieve realistic timing results.

When IBM last year announced the tool, the company said it would offer it commercially to all comers and that it would be fab-independent. Is that still the case?

A IBM has enabled EinsTimer statistical timing in a fab-independent manner and has been working with a few clients in this mode. However, IBM's main focus is on providing comprehensive approaches to its technology and platform partners. Regardless of where customers fabricate their chips, IBM offers its clients design services that can take advantage of the company's knowledge and expertise, including statistical timing and optimization.

What are the next steps for the technology? How do you proliferate the technology and get designers not only up to speed on its benefits, but also able to use it on real designs?

A Several parts of the methodology must evolve to take full advantage of the new statistical paradigm: process modeling, library characterization, physical synthesis, and test. Several factors contribute to quick proliferation. First, the tools must be pushbutton and easy-to-use. Second, the timing reports should be intuitive and configurable so that someone schooled in deterministic timing will easily get used to the new reports. Finally, training, education, support, and documentation will play big roles in widespread acceptance of the new tools.

–by Michael Santarini

Outstanding RF performance—at outstanding prices.
In power detection, analog is everywhere.

AD8317
- Operating 1 MHz to 10 GHz
- 50 dB dynamic range
- Better than ±0.5 dB stability over temperature
- 3 mm × 2 mm, 8-lead LFCSP
- Pricing: $3.93/1k USD

AD8318
- Operating 1 MHz to 8 GHz
- 60 dB dynamic range
- Better than ±0.5 dB stability over temperature
- 4 mm × 4 mm, 16-lead LFCSP
- Pricing: $4.99/1k USD

AD8319
- Operating 1 MHz to 10 GHz
- 40 dB dynamic range
- Better than ±0.5 dB stability over temperature
- 3 mm × 2 mm, 8-lead LFCSP
- Pricing: $2.99/1k USD

New log amps extend RF power measurement to 10 GHz

ADI's new log amps redefine the parameters of accurate RF power detection. These detectors support all cellular and broadband wireless standards and other demanding applications up to 10 GHz—enabling designers to address more applications with less time and effort. They also provide performance and value that are unsurpassed in the industry.

From RF to IF, mixers to power detection, for handsets to base stations—analog is everywhere.

ADI—for every part of RF designs

- VGAs
- Modulators
- Demodulators
- Mixers
- Gain blocks
- RF amplifiers
- DDS
- PLL

To order samples and evaluation boards, visit our website.

analog is everywhere.™

www.analog.com/logdetectors

ANALOG DEVICES

GLOBAL DESIGNER

MEMS microphone has digital output

Akustica's claim that its AKU2000 is the first CMOS MEMS (microelectromechanical-system), direct-digital-output, single-chip microphone. The company licensed the technology, which it believes is comprehensively patent-protected, from Carnegie-Mellon University (Pittsburgh). The technology allows Akustica to build MEMS using the metallization layers of a standard-CMOS process to form the membrane that makes the sensing element of the microphone. Because the technology is standard-CMOS, the company can build an output amplifier and fourth-order sigma-delta modulator onto the same chip.

Unlike the electret-capacitor-microphone technology the Akustica product aspires to replace, the chip is surface-mountable in a standard flow-soldering process. It requires a clock input of 1 to 4 MHz and operates from 2.8 to 3.6V, using less than 750 μA. Akustica designed the 4×4-mm package for reflow soldering on the reverse of a pc board. The board must have a through-hole aligned with the membrane opening on the chip, but this arrangement simplifies sealing the assembly to an external surface. The output is a pulse-density-modulated, serial bit stream. Akustica defines the chip's frequency response by a mask that specifies it to be ±3 dB over 200 Hz to 6 kHz.

Akustica initially targets the laptop/notebook-computer market, although the cellular phone is a potentially bigger market. However, the company believes that the standard electret-capacitor microphone is more deeply entrenched in cell phones and that Akustica will be better able to attack that sector when it has driven its product further down the price curve.

The fact that the device has a digital output makes the AKU2000 of great interest to laptop/notebook designers and also those working in a similar physical format. The high impedance and low signal level of an electret make it vulnerable to electrical noise: It is difficult to route screened wiring through a laptop's hinge, so the microphone often resides in the chassis of the machine, close to sources of mechanical noise, such as hard-disk drives and fans. The device's digital output not only overcomes that problem, but also makes it feasible to mount two or four of them on a screen bezel. The designer can use them as a small array to shape the overall acoustic response into a high-sensitivity zone where the user is and cancel out noise from elsewhere. The AKU2000 sells for $3.87 (1000).

—by Graham Prophet, *EDN Europe*

▷**Akustica**, www.akustica.com.

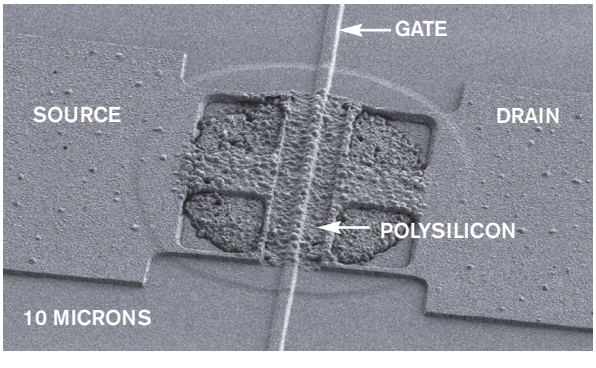
Spin-coating process produces TFT with liquid silicon

Seiko Epson Corp and JSR Corp have jointly developed a silicon film with liquid coating and ink-jet-patterning processes. The silicon film produces a low-temperature polysilicon TFT (thin-film transistor) with performance comparable to that of film using the conventional CVD (chemical-vapor-deposition) method. The new material is a high-order silane compound of hydrogen and silicon that dissolves in an organic solvent.

To get a silicon film, developers spin-coated the material onto a substrate and baked it in an inert atmosphere. The electrons in the process achieve mobility of 108 cm^2/Vsec. Forming a TFT prototype using a silicon-film pattern with the ink-jet method achieves mobility of 6.5 cm^2/Vsec, a better figure than that for spin-coating. Eventual target applications include LCD televisions and ink-jet printers.**—by Tatsuya Ito, *EDN Japan***

▷**Seiko Epson Corp**, www.epson.co/jp.

▷**JSR Corp**, www.jsr.co/jp.



A scanning electromicroscope photo of a sample of Epson's new film coating shows the source, gate, drain, and polysilicon island.

05.11.06

Consortium invests $800,000 for five years

The JEITA (Japan Electronics and Information Technology Industries Association) has announced a new semiconductor-development project, TSC (Tsukuba Semiconductor Consortium). It combines the STARC (Semiconductor Technology Academic Research Center) design-technology company and Selete (Semiconductor Leading Edge Technologies). STARC plans to invest 20 billion yen ($180,000) for five years, and Selete will invest 70 billion yen ($600,000) for five years. Both focus on chip-technology development in process nodes of 45 nm and smaller.

STARC will focus on design for manufacturing, high-level design, and failure diagnostics, and Selete will target metal-gate processes, high-k-gate processes, carbon interconnect, extreme-ultraviolet lithography, and optical interconnect.—by Takatsuna Mamoto, *EDN Japan*

▶**Japan Electronics Information Technologies Industries Association**, www.jeita.or/jp.

▶**Semiconductor Technology Academic Research Center**, www.starc.jp/index-e.html.

▶**Semiconductor Leading Edge Technologies**, www.selete.co.jp/?lang=EN.

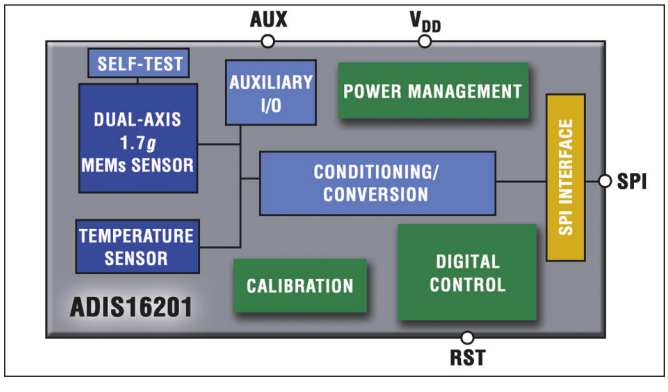
LEADING inside

A series of engineering insights
by Analog Devices.

Highly Integrated, Programmable Single-Component Sensors Solve Problems in Industrial System Design

Sensors have the potential for providing revolutionary improvements in performance, reliability, safety, and cost-of-ownership within industrial system designs. Examples involving inertial sensors include platform stabilization, motion control for industrial machinery, security devices, antenna stabilization, robotics, navigation, mechanical leveling, and many others. However, a gap has long existed between good sensor technology and its implementation within critical industrial systems. Embedding sensor processing within industrial equipment typically requires that the designer have intimate knowledge of the sensor technology to design and implement a signal chain that properly tunes and calibrates a given sensor for its application. For inertial sensors, this typically also requires the capability for motion testing. The system expense of this implementation has created a barrier to more rapid sensor deployment, particularly for customers and applications with moderate production volumes. The problem is worsened by the physical limitations posed by some applications (for instance, embedded vibration analysis) where extreme density, environmental conditions, and remoteness have pushed requirements beyond what is available in standard sensor and signal conditioning components.

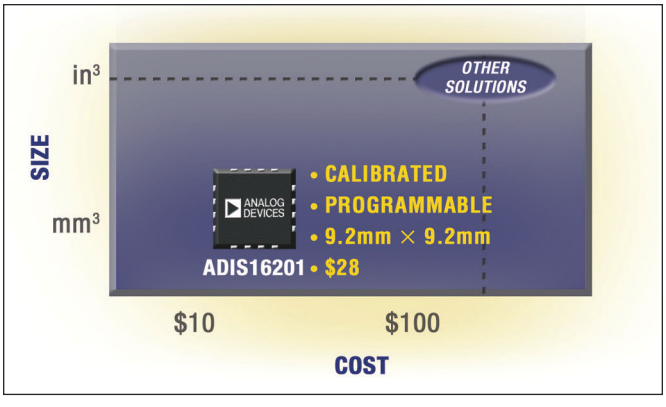
The Analog Devices' *i*Sensor™ product family was created in recognition of this gap in industrial sensor applications. The ADIS16201 *i*Sensor is the first implementation of a new patent pending single-package integration technology. It's the world's first direct output, linear-in-degrees inclinometer that is available as a single component. Incorporating a complete sensor and data processing signal path, the device is both a fully functional programmable dual-axis accelerometer and a dual-axis inclinometer.



A complete dual-axis acceleration and inclination angle measurement system in a single, compact package.

The ADIS16201 provides a gain and offset variability of less than 1%, reduces voltage and mechanical mounting sensitivities, and provides a simple single command interface which allows in-system auto-zero calibration.

It also includes several embedded features, including programmable sample rate, digital filtering, power management, configurable alarms, auxiliary analog and digital I/O, and self-test. This eliminates the need for external circuitry and enables a much simplified system interface, all controlled via an SPI port. Sensor outputs include two axes of ±1.7 *g* acceleration, two axes of ±90° inclination (with accuracy within 0.25°), and temperature. Previously, the same functionality and performance could only be found in devices more than 100× larger, and 10× more costly. The ADIS16201 is available in a small 16-lead laminate-based land grid array (LGA) package, at 1k unit pricing of $28.

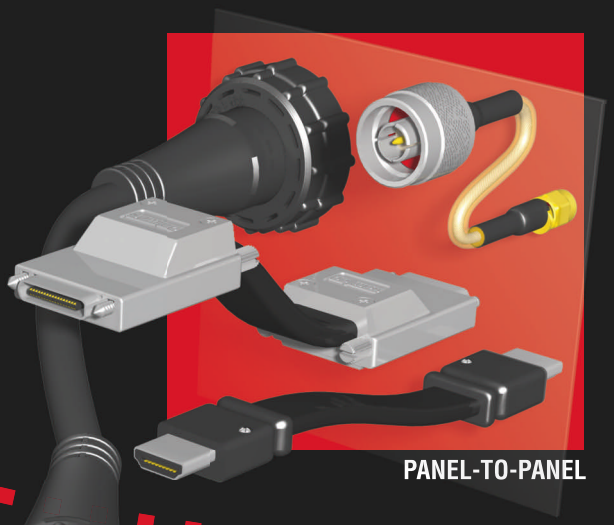


With up to 100x size reduction and 10x cost reduction, the ADIS16201 brings embedded sensing to a broader base of customers and applications.

*i*Sensor integration eliminates a key barrier to the advancement of sensor applications in the industrial market by offering unprecedented functionality, programmability, and simplicity to the system designer. The standard programming interface also allows the user to easily tailor the devices to the application, and very quickly move through prototyping, evaluation, and implementation. Now in development are additional *i*Sensor products targeted at embedded vibration analysis and programmable angular rate sensing. For additional product information, visit *www.analog.com/iSensors.*

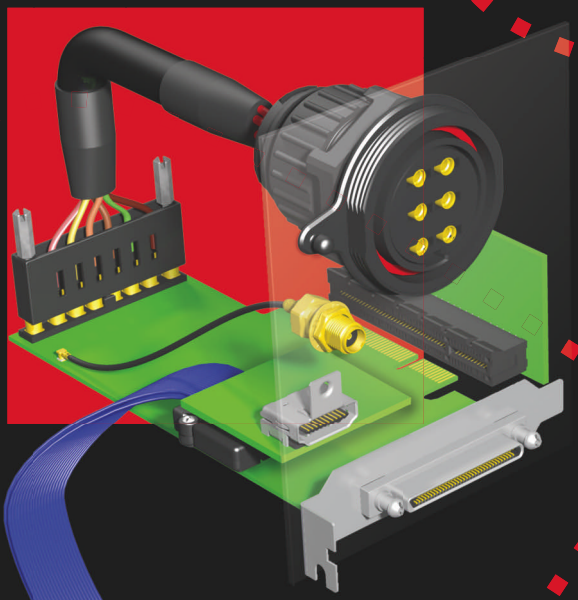
Author Profile: ***Bob Scannell*** *is the business development manager for the iSensor product strategy at Analog Devices.*

SIGNAL INTEGRITY



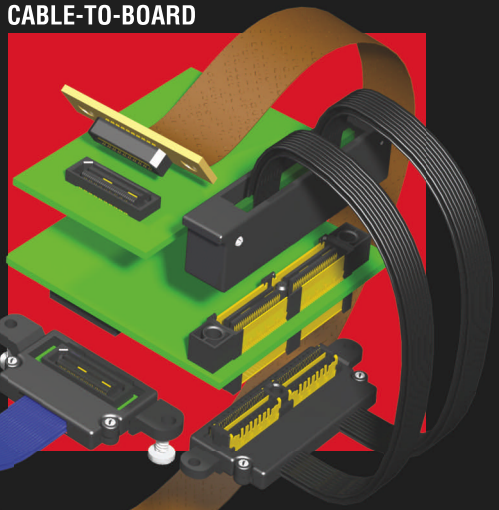
PANEL-TO-PANEL

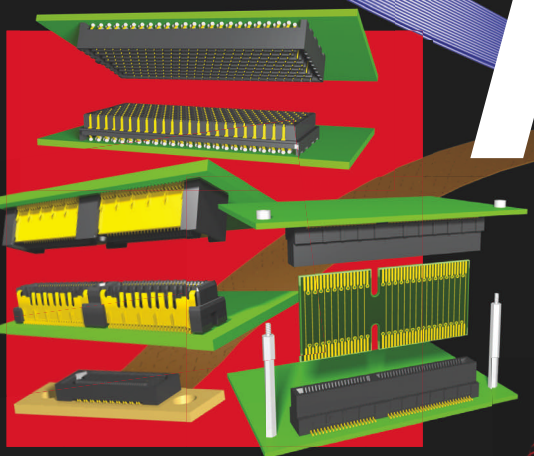
PANEL-TO-BOARD



FROM THE OUTSIDE IN

CABLE-TO-BOARD





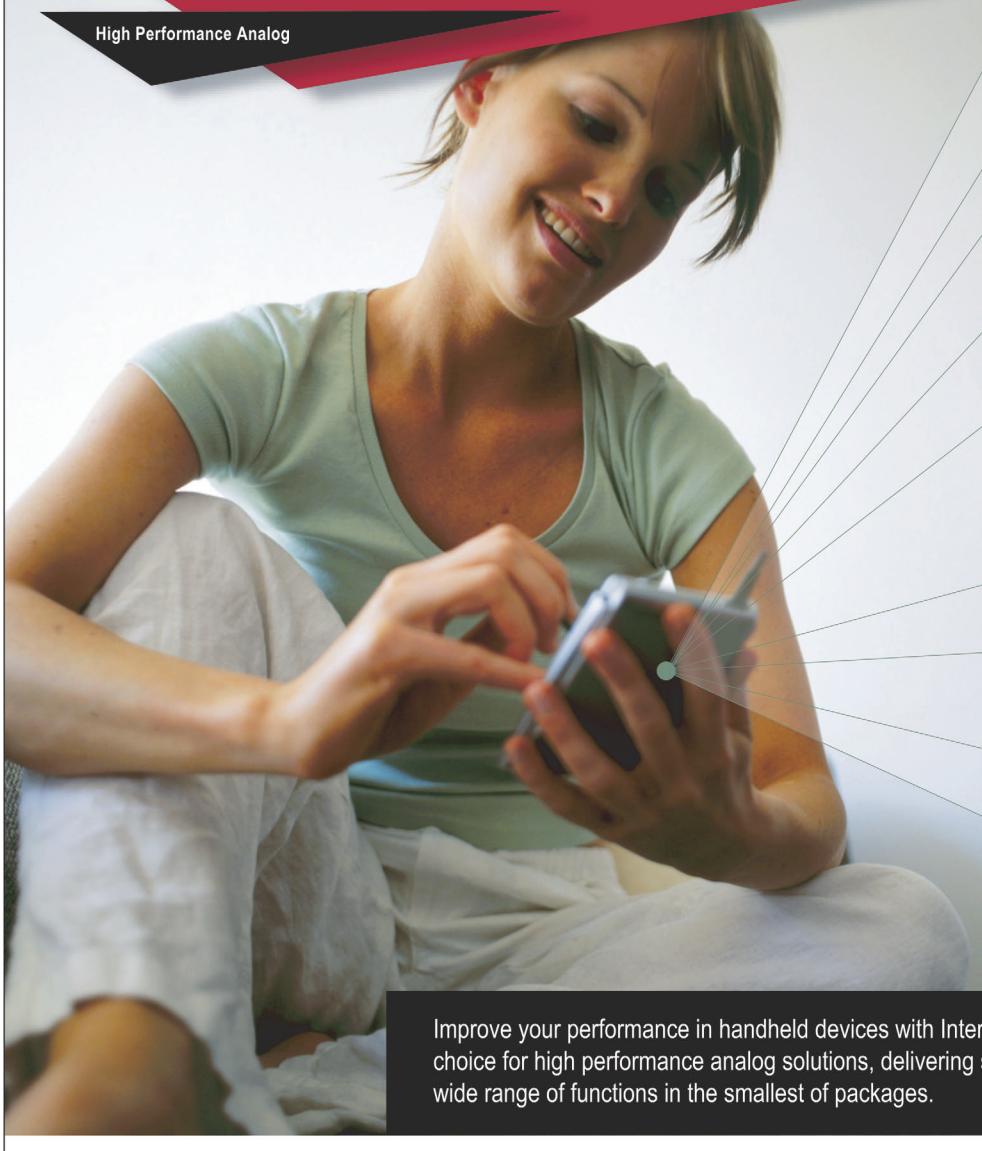
BOARD-TO-BOARD

samtec

www.samtec.com/si

Intersil Handheld Products

High Performance Analog



Analog Switch
- ISL8484
- ISL8499

Battery Authentication
- ISL6296

Battery Management
- ISL6294
- ISL6299

Composite Video
- ISL59110
- ISL59111

Core Power
- ISL6273
- ISL6274
- ISL9000
- ISL9200

Fuel Gauge
- ISL6295

Light Sensor
- EL7900
- ISL29000

Voltage Reference
- ISL60007

Improve your performance in handheld devices with Intersil ICs. Intersil is your first choice for high performance analog solutions, delivering superior performance for a wide range of functions in the smallest of packages.

- Analog Switches
- Battery Management
- Battery Authentication
- Composite Video Drivers
- Core Power
- DCPs
- Image Buffers
- Ambient Light Sensors
- Memory Power Mangement
- Voltage Reference

Intersil's innovative handheld products include everything form complete power management to an ultra-small video driver that enables high-quality video output directly from a handheld device. We've even got backlight and ambient light sensors that combine efficient power usage along with superior usability and display.

To see all the different functions Intersil supports in handheld products go to **www.intersil.com/applications** and see the latest high-end consumer application block diagrams available.

Complete Handheld Products Linecard is available at **www.intersil.com/handheld**

Datasheets, free samples, and more information available at **www.intersil.com**

1001 Murphy Ranch Road,
Milpitas, CA 95035
North America 1-888-INTERSIL
International (01) 1-321-724-7143

Intersil – An industry leader in Switching Regulators and Amplifiers.

intersil®
HIGH PERFORMANCE ANALOG

BY BONNIE BAKER

Charge your SAR-converter inputs

It is tempting to drive a SAR (successive-approximation register) ADC with just an amplifier. As an added benefit, you might try to configure the amplifier circuit in a gain or antialiasing-filter stage. These enhancements seem reasonable as you try to optimize your device use. However, did you think about whether you would compromise the effectiveness of your op-amp/converter pair (**Figure 1**)?

If you need good, accurate performance at dc as well as ac, regardless of your throughput rate, the analog-input stage of the SAR ADC requires special attention. The model of the input stage of most modern ADCs is a resistor/capacitor pair with two switches and a voltage source (**Figure 2**). The resistance, R_{SW}, in the converter's input is the closed-switch resistance. This switch closes during the acquisition time of the conversion process and opens during the conversion time. The converter uses capacitance, C_{SH}, which is the total of the distributed on-chip capacitance, for the input-signal-sampling process.

First and foremost, you need to give sample capacitor C_{SH} enough charging time to reach at least $^1/_2$ LSB of the final value. Theoretically, for a 12-bit converter, enough time would be more than eight times $R_{SW} \times C_{SH}$. Given error margins and component variations, you should use multiples of 10 to 15. The SAR converter needs an op amp with a gain of ±1V/V, along with an R_{IN}-C_{IN} external resistor/capacitor pair. During sampling, the ADC uses capacitor C_{IN} for signal stability. Resistor R_{IN} isolates the amplifier from the ADC's load capacitance. The op amp isolates the ADC from high-impedance loads and drives C_{IN} and C_{SH}, facilitating a quick charge time while the ADC is sampling.

Design this seemingly simple circuit with the following guidelines. C_{IN} is a silver mica or C0G dielectric-type capacitor. These types of capacitors provide stability to the voltage and frequency coefficient of C_{SH}. Capacitors such as X7R, Z5U, and others have significant voltage and frequency "memory" and might degrade the converter's total-harmonic-distortion performance. At a minimum, the value of C_{IN} is greater than 20 times C_{SH}. You determine the value of R_{IN} using the ADC internal resistor and capacitor values. The time constant of the final values of C_{IN} and R_{IN} is 70% of the C_{SH}/R_{SW} time constant, with a value of $50\Omega < R_{IN} < 2\ k\Omega$. Finally, the op-amp circuit, with C_{IN} and R_{IN} installed, should be able to settle to your converter's resolution and still drive a step-response signal. You can prove this function with bench testing (**Reference 1**).

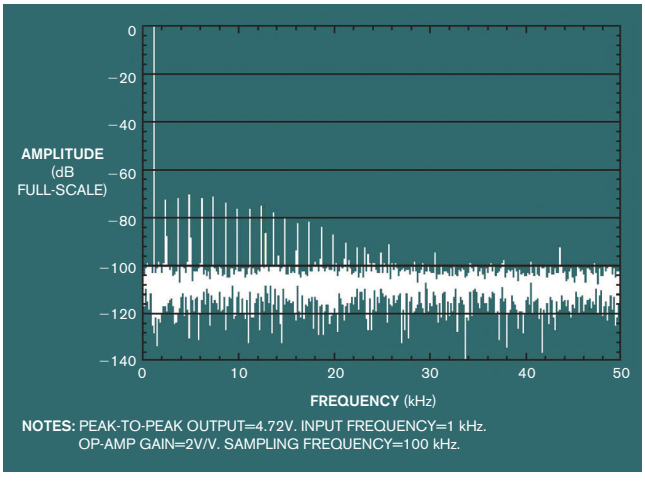


Figure 1 An improperly driven, 12-bit SAR ADC can produce unwanted noise and harmonic distortion. In this diagram, the SNR (signal-to-noise ratio) is 69.76 dB full-scale, and the THD (total harmonic distortion) is −63.34 dB full-scale for a converter that performs at an SNR of 71.82 dB full-scale and a THD of 78.82 dB full-scale.

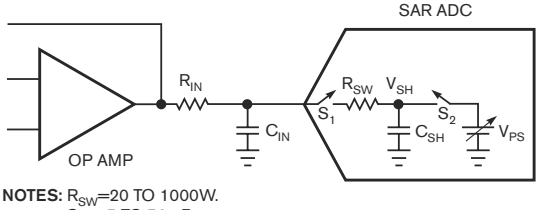


Figure 2 The input structure of a SAR converter initially has a sample-and-hold capacitor, C_{SW}, following a switch, S_1, which controls the sampling time.

REFERENCE

1 Oljaca, Miro, and Bill Klein, "Optimizing the High Accuracy Measurement Circuit ... ," PCIM conference proceedings, 2004.

MORE AT EDN.COM

For additional references, visit the Web version of this column at www.edn.com/060511bb.

Bonnie Baker is the author of A Baker's Dozen: Real Analog Solutions for Digital Designers. *You can reach her at bonnie@ti.com.*

In distress about the approaching deadline? The right data can set you free.

RoHS COMPLIANT

ELECTRICAL & CIRCUIT PROTECTION

INTERCONNECT PRODUCTS/ WIRE & CABLE

LAMPS & DISPLAYS

OPTOELECTRONICS

PASSIVES

POWER PRODUCTS

SEMICONDUCTORS & PROTOTYPING

TEST & MEASUREMENT

TOOLS & PRODUCTION SUPPLIES

Supplier Authorized Distributor

RoHS Compliant

Use our free RoHS BOM Data Service.

At Newark InOne, we'll "scrub" your parts list or bill of material for prototype or small production needs against our database of 4 million parts, identifying which of your parts are compliant, which are changing, and the number and kinds of substitutes available.

Securely upload your parts list at www.newarkinone.com/bom or call 1.800.463.9275 today.

NEWARK inone®

PRY FURTHER AT EDN.COM

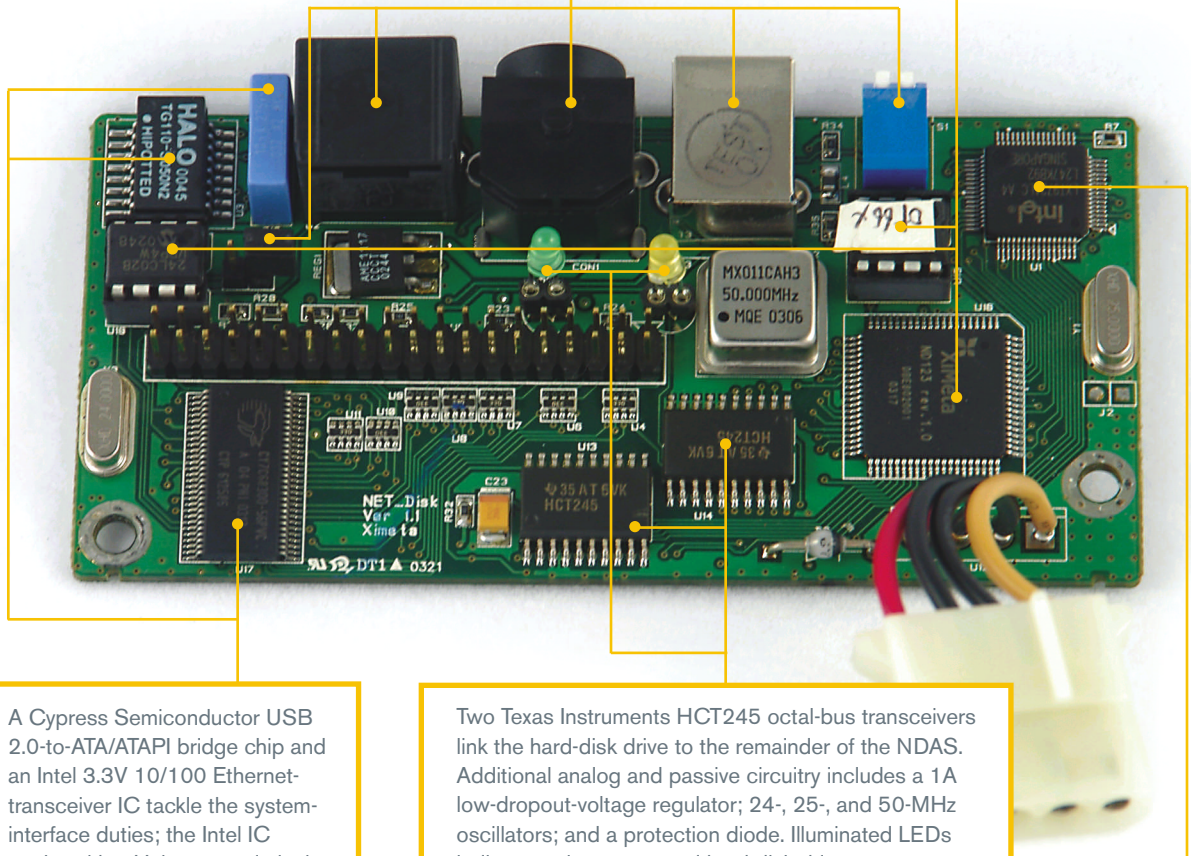
For expanded analysis and additional internal pictures of two first- and second-generation Ximeta NetDisks, visit www.edn.com/060511pry.

NDAS undressed: dissecting a NAS substitute

Ximeta's NDAS (network-direct-attached-storage) NetDisks sell for less than "pure" NAS (network-attached-storage) drives. To do so, they shift some of the processing burden to the PCs that connect to them. What's inside the enclosure, and how does the parts list differ from what you'd find in a fuller-featured alternative?

Back-panel connections support USB, wired-Ethernet, and dc power. First-generation units relied on user-controlled manual switches to toggle between USB and Ethernet; second-generation devices automatically select the proper system connection. A pc-board-mounted jumper is also missing from the second-generation device.

A NAS incorporates a stand-alone or core-in-SOC (system-on-chip) microprocessor, running an operating system such as Linux, along with many dozens or hundreds of megabytes of nonvolatile and volatile system memory. NDAS makes do with a proprietary 80-lead TQFP ASIC, whose myriad functions you can decipher at www.ximeta.com/files/01453436.pdf, along with socketed 2- and 16-kbit serial EEPROMs. The 16-kbit EEPROM sports a handwritten ROM-code sticker.



A Cypress Semiconductor USB 2.0-to-ATA/ATAPI bridge chip and an Intel 3.3V 10/100 Ethernet-transceiver IC tackle the system-interface duties; the Intel IC works with a Halo magnetic-isolation module and Pilkor 275V-tolerant, electromagnetic-interference-suppressing capacitor.

Two Texas Instruments HCT245 octal-bus transceivers link the hard-disk drive to the remainder of the NDAS. Additional analog and passive circuitry includes a 1A low-dropout-voltage regulator; 24-, 25-, and 50-MHz oscillators; and a protection diode. Illuminated LEDs indicate active-power and hard-disk-drive accesses.

RACE TOWARDS THE NEXT AUTOMOTIVE NETWORK WITH THE NEW FLEXRAY, CAN, LIN, AND IDB-1394 CONTROLLERS.

Fujitsu's new FlexRay controller enables X-by-Wire technology for in-vehicle networks. This application-specific standard product complements all of the existing standard automotive buses including CAN and LIN. Based on Bosch IP, this next-generation controller delivers 10 Megabits per second over two channels and provides fault-tolerant, deterministic transmission, suitable for the engine control, braking and steering subsystems now being introduced using the FlexRay protocol. Fujitsu is committed to developing FlexRay embedded microcontrollers for further integration.

For more information, call **(800) 866-8608** or visit **http://us.fujitsu.com/micro**

FLEXRAY

- The world's first controller based on FlexRay version 2.0 standard and on track for version 2.1
- Configurable parallel interface

MICROCONTROLLERS

- 8-bit, 16-bit, 32-bit MCUs
- Up to 6 CAN supports, 128 messages per channel
- Multiple serial interfaces (CAN, LIN, I^2C, SIO, UART)
- High-speed and multiple A/D conversion units

FUJITSU

THE POSSIBILITIES ARE INFINITE

Microsoft

Real-time monitoring for critical patient care. That's the Power of Windows Embedded.

Getting real-time patient monitoring devices into the hands of doctors and nurses can save lives. That's why the engineers at Zoe Medical chose the speed and reliability of Windows CE to develop their Nightingale Personal Patient Monitor (PPM2) and make it available to hospitals in just 12 months.

With only two developers and a short timeframe, Zoe Medical took advantage of the shared source code in Windows CE to move its applications from its traditional MS-DOS platform to a system that is more flexible, familiar, and provides the graphic and audio support its customers demand. Plus, the hard real-time performance of Windows CE met the strict requirements of the PPM2 to monitor and communicate vital patient functions as they happen.

"We took two critical patient care devices to market in only a year. Windows CE was a big part of that achievement." — JIM CHICKERING / **Clinical Applications Manager** / Zoe Medical Development

The Power to Build Great Devices—get it with **Windows CE, Windows XP Embedded,** or **Windows Embedded for Point of Service.**

www.learnaboutembedded.com/monitor

Windows Embedded

BY DAVID LOHBECK • NATIONAL INSTRUMENTS

Hazardous-voltage primer

UNDERSTANDING THE HAZARDS ASSOCIATED WITH VOLTAGE AND KNOWING THE PRINCIPLES OF SAFETY AND THE IMPORTANCE OF CERTIFICATION ARE THE KEYS TO SAFE DESIGN AND PRODUCT USE. EVEN LOW VOLTAGE IS HAZARDOUS AND CAN DAMAGE PRODUCTS AND HARM USERS.

It is common knowledge that wall-outlet voltages of 120V in the United States and 230V in Europe can cause severe shock or death, but did you know that many people consider 120 and 230V to be low-voltage? Believe it or not, according to most standards, voltages less than or equal to 1000V are low. Voltages greater than 1000V are high and are not commonplace in the typical home or workplace. More specifically, peak voltage greater than 42.4V is hazardous; voltage less than or equal to 42.4V, or SELV (safety extra-low voltage), is nonhazardous. It is difficult to know when electricity can cause serious injury or be fatal. Contact for only 1 to 3 sec with currents of only 6 to 200 mA can cause electrocution by disrupting the normal rhythm of heart muscles, resulting in fibrillation and leading to death. An example of how little voltage or current it takes to electrocute a person is the 120V/15W nightlight. Drawing 125 mA, this seemingly innocuous everyday object has enough voltage and current to put it well within the danger zone. **Table 1** lists the standard ranges for low and high voltages.

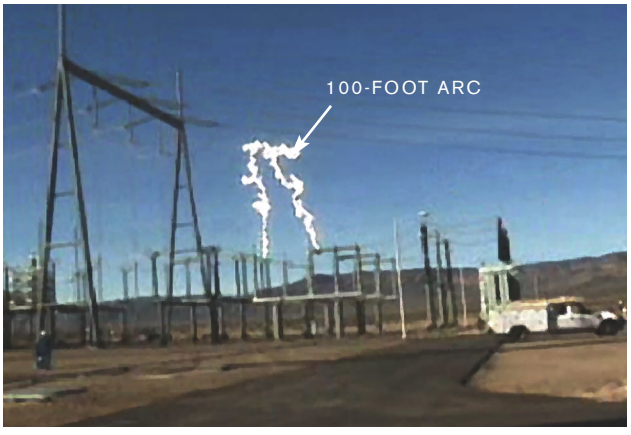


Figure 1 A switch failure at the Eldorado substation in Boulder City, NV, sent this 100-foot long, 500-kV arc into the air (courtesy Stoneridge Engineering, www.teslamania.com).

TABLE 1 VOLTAGE TERMS AND VALUES

Range	Voltage term[1]	Value[1]	Description
Low	Safety extra-low voltage[2]	≤42.4V peak or ≤60V dc	"Safe," user-touchable secondary circuit designed and protected to remain under safe voltage levels in normal operation and under single fault; double insulation
Low	Extra-low voltage[2]	≤42.4V peak or ≤60V dc	Secondary, nontouchable circuit separated from hazardous voltage by basic insulation; not safety extra-low voltage or limited-current circuit and not fault-tolerant
Low	Low voltage[3]	≤1 kV ac	"Hazardous-voltage" circuit, such as primary circuit connected to low-voltage-mains supply, such as 120/230V ac[6]
High	Medium voltage[4]	>1 kV ac to 100 kV ac	"Distribution grid" from substations distributed to residences and commercial buildings
High	High voltage[4]	≥100 kV ac to ≤230 kV ac	"Transmission-grid" long-distance transmission-line voltage with typical maximum distances of approximately 300 miles (483 km)
High	Extra-high voltage[5]	>230 kV ac to ≤800 kV ac	"Transmission-grid" long-distance transmission-line voltage with typical maximum distances of approximately 300 miles (483 km)
High	Ultrahigh voltage[5]	>800 kV ac to 2 MV ac	"Transmission-grid" long-distance transmission-line voltage with typical maximum distances of approximately 300 miles (483 km)

[1]Terms and values are for illustration and may vary between standards.
[2]IEC 60950-1 and other standards.
[3]NEC-NFPA 70 low voltage=600V; ANSI/IEEE low voltage=1 kV ac; European Union's Low-voltage Directive: low voltage 50V to 1 kV ac, 75 to 1500V dc.
[4]ANSI C84.1 and IEEE 100.
[5]IEEE 1312 and IEEE 100.
[6]Hazardous voltage is greater than 30V rms and 42.4V peak or 60V dc. Test-and-measurement products are greater than 33V rms and 48.7V peak or 70V dc. National deviations may exist.

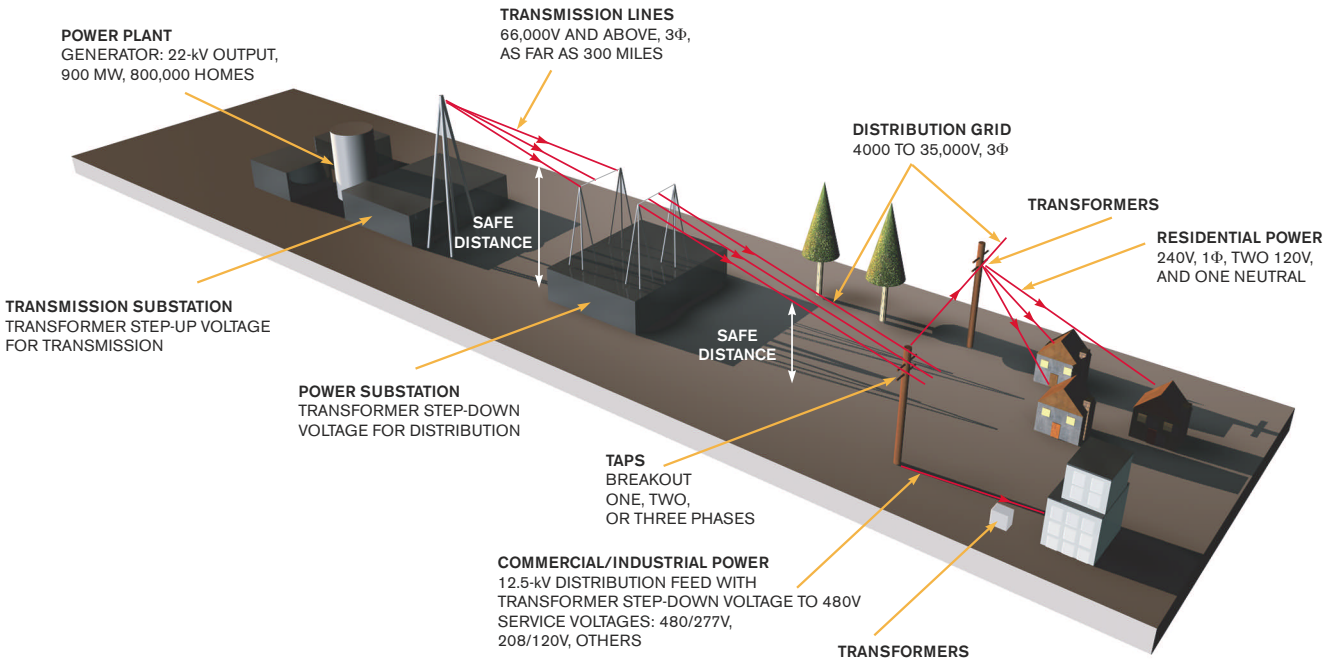


Figure 2 The typical power-distribution system includes multiple voltage levels and transmission standards.

Electricity kills or injures more than 1000 people a year in the United States. Voltages of 100 to 250V ac in wall outlets are the most common and can be lethal. This voltage range can cause significant current flow through the body. Outdoor electricity involves high voltages in which the duration of contact can be significant enough to cause deep burns and cardiac arrest. Electrical current travels at the speed of light, approximately 186,000 miles/sec, and follows the path of least resistance to ground. The human body is approximately 70% water and makes an excellent conductor. Human-body resistance varies depending on how well you are grounded, your age, your size, and your gender. The amount of perspiration on your body also affects your resistance; more perspiration increases your vulnerability. To illustrate how a 120V wall-outlet voltage can affect a person, you divide the 120V voltage by the resistance to yield the current. For a high body resistance, dividing 120V by 1 kΩ yields 1.2-mA current. For medium and low body resistance, divide the 120V by 10 and 1 kΩ, respectively, yielding 12 and 120 mA, respectively. At 1.2 mA, a human body would be on the threshold of feeling a tingling sensation; at 12 mA, the human body would feel the beginning of a freezing, or "can't-let-go," feeling. At 120 mA, the feeling would be extreme pain and possible ventricular fibrillation.

Current follows the path of least resistance to ground. Arteries, nerves, and muscles have low resistance, whereas bone, fat, and tendons have relatively high resistance. The human brain, heart, and nervous system are the most sensitive. These body parts feel a shock with a current as low as 0.5 mA. For hand-to-foot currents higher than 5 mA, a victim can't free himself from the source. Even if the jolt throws a victim free of the power source, he can go into respiratory arrest, cardiac arrest, or both. Currents greater than 20 mA may deliver a lethal shock (**Table 2**). Jolts higher than 1A throw the heart into a contraction; internal body heating is significant. Thermal burns may result in death or the loss of a limb long after the incident.

TABLE 2 THRESHOLD AND UL LIMITS FOR CONTINUOUS 60-Hz CURRENT AND THEIR EFFECTS

Physiological effect	Reaction	Threshold for continuous 15- to 100-Hz current (mA)	UL-specified limit for continuous 60-Hz sinusoidal current (mA)
Involuntary muscular reaction	Perception level, tingling sensation	0.5	0.51
Inability to let go (tetanized muscle)	Painful shock, freezing current, inability to let go	10	5
Ventricular fibrillation	Heart rhythm affected, death may occur	35	20

Notes:
1. Ordinarily, a limit of 0.75 mA applies to stationary or fixed cord-connected products with equipment-grounding connectors.
2. IEC Publication 479 describes data in the third column.

Highly integrated, streamlined RFID pedestals for portals and beyond.

Our M/A-COM RFID antenna measures 19"x 8"x 3".

This sleek, flexible pedestal design is one more example of Tyco Electronics' leadership in RFID technology. The unit integrates multiple antennas and a portal reader into a single- or dual-sided turnkey solution. It features a small footprint, rugged design, easy installation and service bay for quick access to GPIO, network connections and resets. Unobtrusive, low-profile wall-mounted units are also available. All units are available in worldwide frequency bands with flexible reader mounting configurations.

Tyco Electronics offers a full range of M/A-COM antennas and RF components for any RFID application and can provide value-added engineering and assembly services. To learn more, please contact us at 978-442-4000 or www.macom.com/rfid

M/A-COM high-performance, small-size components are ideal for all types of readers.

North America 800-366-2266 • Europe +44-1908-574-200
• Asia +81-44-844-8296 • www.tycoelectronics.com

a vital part of your world

tyco Electronics

The factors that determine the severity of an electrical hazard and its effect on the human body are voltage, current, resistance, frequency, duration, and pathway. Voltage forces current to flow, which can damage the heart or brain or cause involuntary muscle contractions. Current determines the extent of the damage and can cause heating of external and internal human-body tissues and organs. Human-body resistance varies depending on how dry or moist the body is and on the current's path through the body. Current passing though the arm generates more thermal damage than through the abdomen because the arm has a smaller cross-sectional area than the abdomen. Frequency also influences the danger; ac causes more ventricular fibrillation than dc, but both can lead to injuries. Duration affects the severity of heating human tissues and organs; the longer the contact, the greater the damage. A 60% chance of mortality exists for a hand-to-hand current pathway through the heart, and 20% mortality exists for a hand-to-foot path. An old adage says to place one hand in your pocket when working near hazardous electricity so that current does not pass through your chest. A better recommendation is not to touch hazardous voltages!

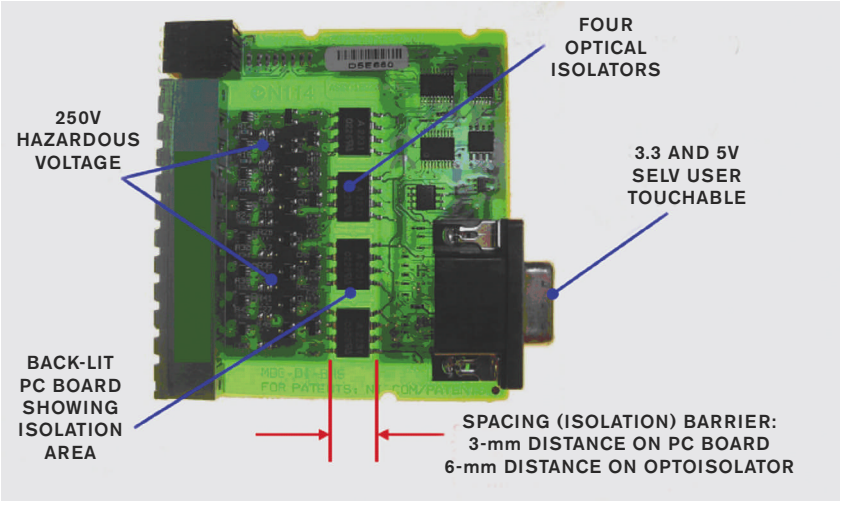


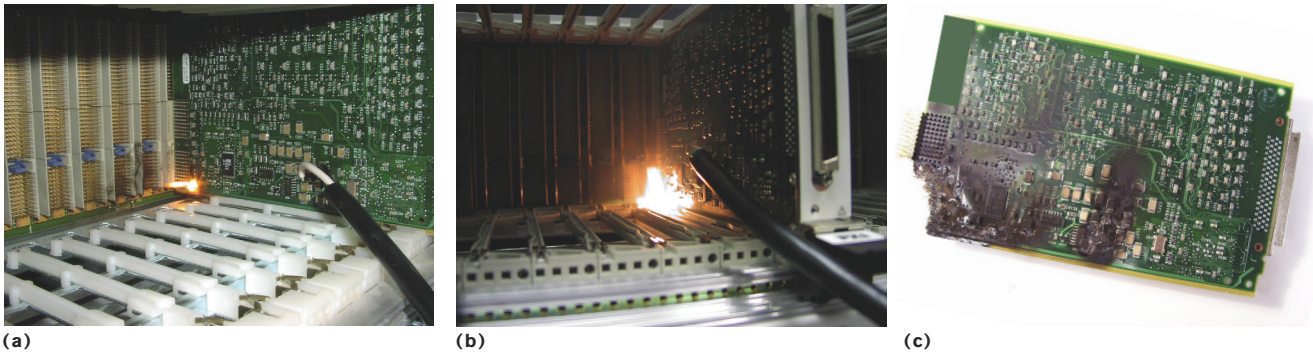
Figure 3 If a capacitor short-circuits in the 5V-dc circuit of a pc-board assembly, the voltage is safe, and the current is only 0.5 mA during normal operation.

Electrical injuries can result from direct contact with electrical energy; electricity arcs, or "flashover," through the air to a person or object; burns from hot surfaces or burning materials; and muscle contractions or startled reactions from falling, dropping a product, or similar scenarios. Direct contact with electricity is the most obvious and commonly encountered danger. Direct contact occurs when someone touches a hazardous, or "live," voltage: greater than 30V rms and 42.4V peak or 60V dc. Proper insulation and distance help protect people from direct contact.

Electricity arcs emanate from lightning strikes, motor start-ups, and line surges. Staff at the Eldorado substation (Boulder City, NV) captured one such extra-high-voltage electric arc. When one of two switches fails to open, an air break switch opens "hot," resulting in a 500-kV arc more than 100 feet long (**Figure 1**). Burns come from surfaces heated by excessive current flow. Touchable surface limits are typically 70°C (158°F) for metals and 80°C (178°F) for plastics. Excessive power consumption can also generate enough heat to cause a fire that expands beyond the product to its surroundings.

POWER DISTRIBUTION AND SAFE DISTANCE

Electricity starts at a power plant with nuclear reactors or steam turbines burning coal, oil, or natural gas to drive the plant generators. These generators provide three-phase ac power that steps up to high voltage for long-distance transmission, and power substations step down the transmission voltages for the distribution grid. The grid distributes three-phase medium voltage, which typically ranges from 4 to 35 kV. Finally, transformers step down the distribution voltage to less than 1 kV for use in



(a) (b) (c)

Figure 4 Without proper current limiting, a shorted capacitor in the 5V-dc circuit of a pc-board assembly can start a fire within seconds (a). After 30 sec, the fire has caused considerable damage (b), destroying the pc board and connector (c).

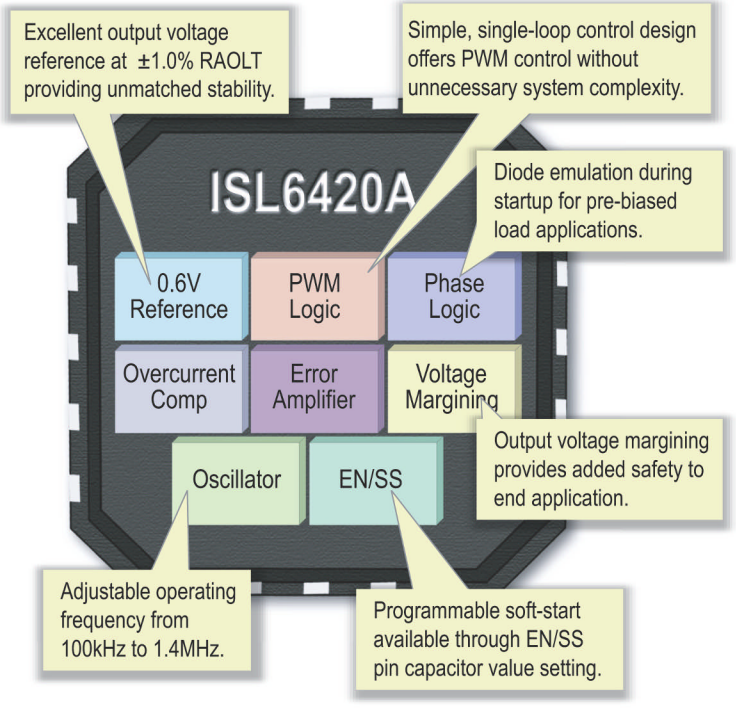
Intersil Switching Regulators

High Performance Analog

Finally... a Step Down That Meets Everybody's Needs

Intersil knows that different applications have different design needs. That's why we've created the ISL6420A wide V_{IN} Step Down Controller. In addition to the flexibility to support multiple input voltages, this device combines control, output adjustment, monitoring and protection into a single package.

The ability to address a wide input voltage range of 4.5V to 28V gives the ISL6420A unmatched flexibility for use in most general purpose applications. It also has resistor-selectable switching frequency from 100kHz to 1.4MHz. Add all this up and Intersil has made choosing the right switching regulator for your design...well, like a day at the beach.



Key Features:

- Operates from 4.5V to 28V input
- Excellent output voltage regulation with 0.6V internal reference with ±1.0% ROALT
- Resistor-selectable switching frequency from 100kHz to 1.4MHz
- Voltage Margining and External Reference Tracking
- Output can sink or source current
- Lossless, programmable overcurrent protection using upper MOSFET's rDS(on)
- Programmable soft-start
- Simple single-loop control design
- Fast transient response
- High-bandwidth error amplifier
- Full 0% to 100% duty cycle
- P_{GOOD} with programmable delay enables integrated supervisory function

Datasheet, samples, and more information available at **www.intersil.com**

Intersil – Switching Regulators for precise power delivery.

intersil®
HIGH PERFORMANCE ANALOG

Figure 5 Product-certification marks are independent, third-party evidence of compliance and are mandatory in some localities.

homes and commercial buildings. In some areas, the distribution lines are underground with transformers typically above ground (**Figure 2**).

The wires on the large steel towers are transmission lines. Extra ground wires sometimes run along the tops of these towers in an attempt to attract lightning, so that it does not travel to the grid and buildings' electrical installations. Distribution lines are at the top of the poles running along roads and are easy to spot because they hang between porcelain insulators. Taps on these poles break out one, two, or three lines to run in different directions. Ground wires running between poles connect to a bare grounding wire that runs down each pole, which is buried six to 10 feet into the earth. Additional wires lower on these poles provide connections for phone, cable TV, or other purposes. Power lines are noninsulated, and what appears to be insulation on some wires is only weatherproofing. Towers and poles separate people and structures from dangerous power lines. The minimum safe distance from persons and structures to power lines is 3m.

GENERAL PRINCIPLES OF SAFETY

Applying the general principles of safety and meeting safety standards are the minimum requirements for compliance with safety laws and meeting consumer expectations. Engineers should design products that meet safety principles, standards, and the latest state of safety technology. Sometimes, product designs must exceed safety standards, such as in cases in which standards do not cover technologies, materials, or construction methods or industry practice has identified a new safety principle. Product designers must consider normal operating conditions as well as likely fault conditions, consequential faults, foreseeable misuses, and external influences, such as temperature, altitude, pollution, moisture, and overvoltages.

The principles of safety are safe design, protective measures, and warnings. You should specify safe design and construction criteria that eliminate or reduce hazards as much as possible. If you cannot implement safe design and cannot eliminate the risks, take the necessary protective measures, such as employing guarding or protective devices. After you have exhausted all other means, inform users of any shortcomings using warnings about residual risks and the need for safeguards, such as training and personal-protection equipment.

When designing products for safety, designers must consider both users and service persons. Typically, users have no access to the hazards that exist in service-access areas, such as behind secured covers. Users are not trained to identify hazards and do not intentionally place themselves in a hazardous situation. Service persons are trained to avoid injury from obvious hazards but should still be protected against unexpected hazards. Manufacturers can achieve this goal by locating parts requiring service away from electrical and mechanical hazards, providing guards to limit accidental contact, and providing warnings or instructions to caution personnel about residual risks. They can place service warnings on the product or document them, depending on the likelihood and severity of injury.

User instructions should focus on avoiding misuse and situations likely to create hazards, such as connection to wrong power source and incorrect fuse replacement. User warnings indicate that a product has some residual risks. Some manufacturers misunderstand when they should apply warnings and use them in place of safe designs. User warnings may be unjustified and therefore violate safety standards and laws, such as when safe design is possible or when a standard does not permit a warning. Safe design is the highest priority and the best way to protect users and ensure that a product remains safe during normal operation, under fault conditions, and with foreseeable misuse.

Users must be safe during reasonably foreseeable misuse, which is use of a product in a way the manufacturer did not intend but could have predicted as a consequence of human behavior. For example, products must remain safe even if a user sets adjustments, knobs, or controls in a way that differs from the instructions. Manufacturers must consider or foresee how a user could misuse a product and design products that are safe in such cases, not relying on user warnings to limit the manufacturers' liability.

Products must provide protection against electric shock and fire risk during normal operation and during a fault. Some products use power supplies with high-power outputs, which, when a fault occurs, can cause current to increase dramatically. For example, if a capacitor short-circuits in the 5V-dc circuit of a pc-board assembly, the voltage is safe, and the current is only 0.5 mA during normal operation (**Figure 3**). However, current rises to more than 20A after the capacitor fault occurs, starting a fire within seconds on the pc board (**Figure 4**). The fire extinguishes itself in a couple of minutes. You can imagine what damage could occur in only a couple of minutes if the fire spread outside the product. It is important to evaluate all electrical circuits and to design products with fusing or circuit breakers to limit shock and fire hazards (**references 1** and **2**).

PRODUCT CERTIFICATION

Standards developers write most specifications out of concerns for the safety of life, property, and the environment.

Intersil Battery Charger ICs

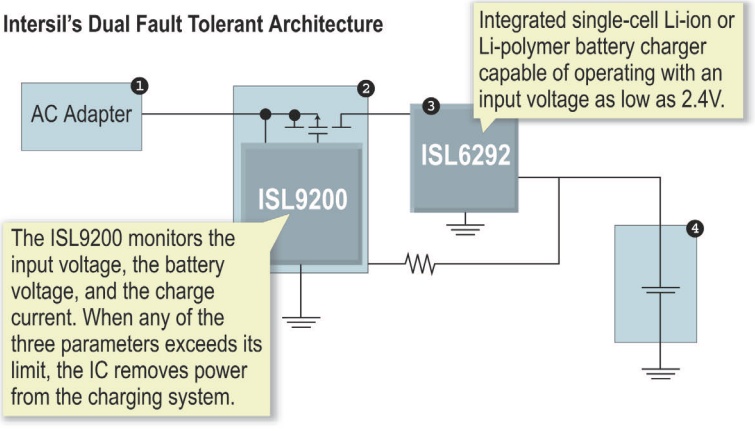
High Performance Analog

The Scariest Thing Inside Your Handheld Should Be Your Pictures

There **is** a real monster out there. Protect your customers from the onslaught of counterfeit and non-OEM battery packs with Intersil's innovative Dual Fault Tolerant charging system. Our integrated triple-level protection approach reduces components and cost while improving design flexibility and system reliability.

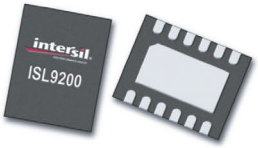
The ISL9200 is a Fault Protection IC optimized to provide redundant safety protection in Li-ion battery charging systems. Together with the ISL6292 Battery Charger IC, Intersil's integrated battery charging system will keep even a counterfeit battery within safe operating limits.

Intersil's Dual Fault Tolerant Architecture



Dual-Fault FMEA (Failure Mode and Effects Analysis)

POTENTIAL FAILURES				Consequence of Dual Failure
❶	❷	❸	❹	
●	●			❸ will fail but the protection module in the battery pack will protect the battery cell.
●		●		Both ❷ and ❹ will protect the battery cell.
●			●	❸ will limit the battery voltage. ❷ has an additional level of protection.
	●	●		The protection module in the battery pack protects the cell.
	●		●	❸ will limit the battery voltage to 4.2V, within 1% error.
		●	●	❷ will sense an over voltage case and remove the power from the system.



- User programmable overcurrent protection threshold
- Input overvoltage protection in less than 1µs
- Battery overvaltage protection
- High immunity of false triggering under transcients
- High accuracy protection thresholds
- Warning output to indicate the occurrence of faults
- logic warning output to indicate fault and an enable input to allow system to remove input power.
- Small, thermal enhanced DFN package.
- Pb-free and RoHS compliant

Datasheet and more information available at **www.intersil.com.**

Intersil – Switching Regulators for precise power delivery.

intersil®
HIGH PERFORMANCE ANALOG

Product-safety standards and laws require manufacturers to protect users from hazards, including dangers from hazardous voltage. Products must comply with safety standards during normal use, under fault condition, and during foreseeable misuse. The ultimate responsibility for providing safe products lies with the manufacturer. However, if an incident occurs, damages may be sought from everyone in the supply chain. With the increased awareness of safety, the number of incidents has dropped over the past 20 years, but cost per incident has dramatically risen.

The technical and legal aspects of product safety can be rigorous and confusing. It is difficult for anyone but a full-time trained professional to keep up with standards, laws, interpretations, and national differences. Safety engineers evaluate and test products according to recognized standards and industry norms, and, on request, they provide proof of compliance for product suppliers, users, and enforcement authorities.

Europe's CE (Conformité Européenne) marking is a manufacturer's self-declaration symbol and not a third-party certification or approval (**Reference 3**). Product-certification marks, on the other hand, are independent, third-party evidence of compliance (**Figure 5**). Certification marks are mandatory in some locations, such as New York, Los Angeles, and Washington. If a product bears a certification mark, then, with few exceptions, it is generally safe to use when you operate it within its specifications. Certification marks are manufacturers' best proof of due diligence should a product's safety compliance come into question (**references 4** and **5**).

MORE AT EDN.COM

Go to www.edn.com/ms4190 and click on Feedback Loop to post a comment on this article.

With an increasing awareness of the potential dangers that hazardous voltage poses, it is incumbent on manufacturers to consider the general principles of safety. Designers must also understand the relevant safety standards and laws to equip themselves with the necessary tools to design safe products. Product-certification marks provide visible proof of a product's compliance and offer consumers peace of mind (**references 6** through **8**). EDN

REFERENCES

1. Lohbeck, David, "Safety isolation protects users and electronic instruments," *EDN*, Sept 30, 2004, pg 59, www.edn.com/article/CA454635.
2. Lohbeck, David, "Safety Design and Certification For Test and Measurement Products, Part 2," *Evaluation Engineering*, November 2003, www.evaluationengineering.com/archive/articles/1203prodsafe.htm.
3. Lohbeck, David, *CE Marking Handbook: A Practical Approach to Global Safety Certification*, August 1998, Newnes, www.books.elsevier.com.
4. Lohbeck, David, "Safety Certification for the T&M World," *Test & Measurement World*, August 2004, www.reed-electronics.com/tmworld/article/CA439351.
5. Lohbeck, David, "The CE marking: separating fact from fiction," *EDN*, Jan 2, 1997, pg 133, www.edn.com/archives/1997/010297/01df_06.htm.
6. Lohbeck, David, "Safety Design and Certification For Test and Measurement Products, Part 1," *Evaluation Engineering*, November 2003, www.evaluationengineering.com/archive/articles/1103prodsafe.htm.
7. Lohbeck, David, "A review of CE Marking," *Design News*, Sept 23, 1996, pg 212, www.designnews.com/article/CA151162.
8. Lohbeck, David, "Walk the Path to the European CE Marking," *Test & Measurement World*, November 1995, pg 23.

AUTHOR'S BIOGRAPHY

David Lohbeck is a product-safety engineer at National Instruments (Austin, TX). Previously, he worked for Motorola, Dell, and TUV in international product safety, machine safety, and electromagnetic compatibility. Lohbeck has published numerous articles on safety and EMC and was an EDN *Innovation finalist for "Best Contributed Article" in 2004 (***Reference 1***). Lohbeck is also the author of* CE Marking Handbook: A Practical Approach to Global Safety Certification. *You can reach him at dave.lohbeck@ni.com.*

Leading the lighting revolution

Cree XLamp® LEDs

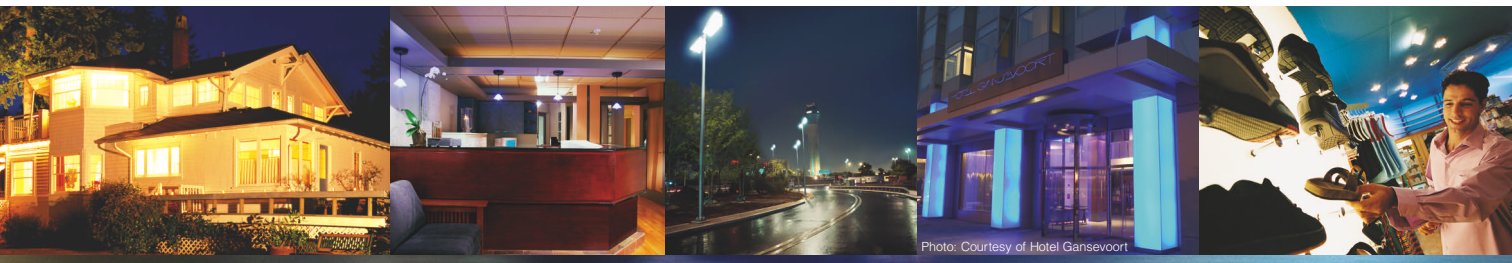


Photo: Courtesy of Hotel Gansevoort

- 47 lumens/watt at 350mA drive current
- Reduced thermal resistance to 8°C/watt
- Available in warm and cool white color temperatures (2700-10000°K)

Cree XLamp 7090 LED

Outperform the rest. Today, Cree delivers the industry's highest performance power LEDs for general lighting applications, with the highest efficiency white light output and the best thermal performance.

To see the future of LED lighting for yourself, visit www.cree.com/xlamp or call 1-800-533-2583 to register for Cree XLamp LED samples, and qualify to receive a Cree XLamp LED flashlight.

CREE® LED Light

Visit Cree at Lightfair International – Booth #1832

BY RON WILSON • EXECUTIVE EDITOR

DESIGNERS CAST A SKEPTICAL EYE ON MIXED-SIGNAL SOCs

THE FUNCTIONS ARE NECESSARY, BUT INTEGRATION CHALLENGES KEEP ANALOG IP OUT OF THE MAINSTREAM FOR SOC DESIGN.

The easiest lesson to draw from the consumer-electronics market is that integration is everything. Mobile beats portable. Palmtop beats mobile, and shirt pocket trumps palmtop. Even in desktop devices, such as game consoles, sleek packaging and low-manufacturing-cost targets depend on ever-higher levels of integration. This trend is not limited to low-cost consumer electronics. Perhaps inevitably, military, automotive, medical, and even industrial applications are demanding the capabilities that consumers want. The integration trend will likely spare only the largest and lowest volume system designs.

But the classic tool of integration, the SOC (system on chip) is running up against a technological barrier. SOCs advance by vacuuming up all the digital functions in a system until there is nothing of significant cost or function left outside the chip. But this approach eventually undermines its own success: When nothing is left to vacuum up, integration is over. Many system designs are approaching that state today. The SOC has absorbed all of the significant digital blocks, leaving only commodity parts, such as mass memory and passive components, with one big exception. Most systems still contain significant cost and functions in precision analog or RF blocks that have remained outside the SOC. Accordingly, these blocks have become the next frontier for SOC integration.

You can already see this trend in such speculative designs as recent "single-chip" cell-phone-handset SOCs from Infineon and Texas Instruments. Such chips include not only the familiar baseband and application processors, but also the analog audio circuitry and the small-signal portion of the RF circuitry. They are not only leading-edge examples of digital integration, but also tours de force in analog and RF integration.

These chips also exemplify what an integrated-device manufacturer can achieve if it has enormous resources; design teams that include analog, RF, device modeling, and process engineers; and an intimate link between the chip-design and process-engineering teams. Ordinary SOC design teams with ordinary skills and resources are not developing these designs. But can they? Can designers bring precision analog or RF blocks into the IP (intellectual-property) assembly-design flow that they have successfully used to create digital SOCs? Or are there barriers, such as inappropriate IP, missing tools, or fundamental issues that will prevent designers from handling analog blocks as black-box IP cores?

THE SOC FLOW

The existence of the digital SOC rests on the ability of its design flow to control complexity. That flow, IP-block assembly, in turn depends upon the existence of previously designed functional blocks that designers can treat almost as black boxes through the early stages of the design cycle. This approach allows behavior-level modeling of the entire chip before designers begin a detailed design, allowing the designers to synthesize, place, and route the individual blocks relatively independently of each other and vastly simplifies the chip-level-verification process. Any experienced SOC designer would state that these processes describe gross oversimplifications of how SOC design actually occurs. However, the IP-assembly flow does significantly reduce design-process complexity compared with treating all of the nets in an SOC with equal attention.

Can designers extend this flow to precision analog or RF circuits? The initial answers from seasoned designers are decidedly mixed. In some simple cases, designers have already done so. For example, some ASIC vendors offer drop-in blocks with low-speed ADCs or moderate-performance PLLs. In other cases, experts say that such an extension to more complex circuits is impossible. "For us, analog design is a matter of constant evolution, not of design reuse," explains Julian Hayes, vice president of marketing for consumer products at Wolfson Laboratories. "IP can provide the foundation for a new design, but it can never be used for cut and paste."

Fundamentally, the digital-IP-integration flow depends on a number of assumptions. First, it assumes that such a thing as reusable IP exists—that a designer can use a block that functions properly in one design for the same function in another design without modification. Second, the methodology assumes that it is possible to model the behavior and timing of a block with acceptable accuracy without understanding the details of its internal function. Third, it assumes that the behavior of a block is independent of the placement and routing of the block and of the internals of signals not connected to it. The problem with precision analog or RF blocks in an SOC flow is simple: They violate each of the assumptions.

REUSABLE IP

An IP-assembly flow can't work if there is no such thing as reusable IP. And many analog experts suggest just that: No analog design is reusable without the intervention of a skilled analog designer. Part of the issue is that nothing in the analog world is analogous to RTL or to synthesis. Designers have attempted to produce analog-synthesis tools, but these tools have for the most part failed, whether through simply not working; working, but only with the intervention of skilled analog engineers; or working only on a narrow range of functions and environment. Today, essentially no analog-synthesis

AT A GLANCE

- Running out of digital functions to integrate, SOC (system-on-chip) designers are starting to eye complex analog and RF functions.
- Analog blocks don't fit into the standard IP (intellectual-property) integration strategy for building SOCs; they have too many interactions with the rest of the design.
- Both using conservative design and having analog experts participate in the integration process are proven solutions to the problem.
- In the future, digitally controlled and self-adjusting analog blocks may serve as black-box functions for SOC designers.

tool is on the market that design teams report they are using.

That lack of availability still leaves open the possibility of hard IP; a designer can drop in a placed-and-routed design unaltered. This approach can work, according to many designers, if the requirements on the block are easy, if the user has sufficient design guidelines to ensure that the circuit stays within its original design space, and if the design has sufficient isolation. But those are big ifs.

A third possibility, which companies including Barcelona Design have explored, is to use a topology to define an analog block and then use automated tools to scale the devices within the topology to meet specifications in an environment. Unfortunately, this approach has not met with great success, either. So, to a first-order approximation, the only reusable analog IP is simple analog IP.

BEHAVIORAL MODELING

To listen to people in the EDA market, you'd think that the mixed-signal-behavioral-modeling problem is the one part of the puzzle that designers have solved. Unfortunately, that is not the story one hears from experienced analog-design teams. For example, Analog Devices may be one of the most advanced design groups in language-based modeling of analog- and mixed-signal circuits. The company has its own internally developed hardware-description language, which can model both discrete- and continuous-time blocks in what engineers describe as C-level abstractions (**Figure 1**). David Robertson, product-line director for high-speed converters at the company, says that it takes a few weeks to a few months to get a current engineering graduate up to speed on the tool. But just knowing how to use the tool is only part of the problem, Robertson adds. "Knowing where to apply it is still an art," he says. In critical situations, modeling still goes right back to the Spice level.

Even vendors of analog IP are skeptical when it comes to accurate behavioral modeling of an analog block. Knowlent Chief Executive Officer Sandipan Bhanot says that, in the analog domain, Spice is still the ultimate court of appeals. "There really isn't anything equivalent to the testbenches, modeling, and measurement languages of the digital domain," he says.

THE DELICACY OF ANALOG

If there has been some progress in design reuse and in high-level modeling of analog or RF circuits, the great issue that remains is independence. Far from being little functional blocks a designer can drop into a design wherever necessary, analog blocks are exquisitely sensitive to their surroundings. One way to think about the problem is in terms of digital and analog netlists. In the digital world, an IP block has inputs, outputs, and power and ground contacts. You assume that any interaction between the block and the rest of the chip takes place on the input- and output-contact points. Most digital flows, at least those below 180 nm, recognize the possibility of capacitive coupling to adjacent routing. However, rather than model these couplings as additional contacts on the block, designers generally ignore them until detailed postroute extraction and then model them as added delays rather than as signal sources or passive networks.

In the analog world, it would be wonderful if that simple model would work. And it can work, assuming that the analog circuit in question is robust to begin with, that it is operating well within its performance envelope, and that the designer has observed sufficiently demanding guidelines with regard to external noise sources, impedances, and isolation. Without those assumptions, the real model of the analog block becomes considerably more complex (**Figure 2**). Even at a behavioral-level view, clock, power, and ground pins become signal paths, not abstract concepts that don't go anywhere. Thus, clock-line cleanliness and supply coupling become fundamental issues that designers must model to determine how the circuit will behave.

This problem is becoming worse, not better. Increasingly, large SOCs are employing aggressive power-management techniques that include clock and

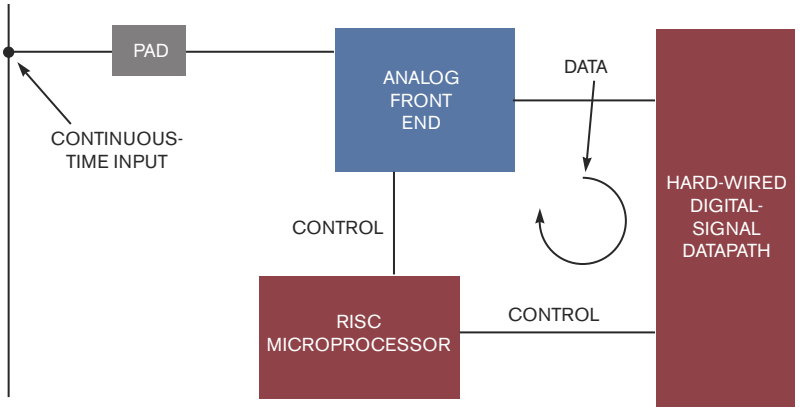
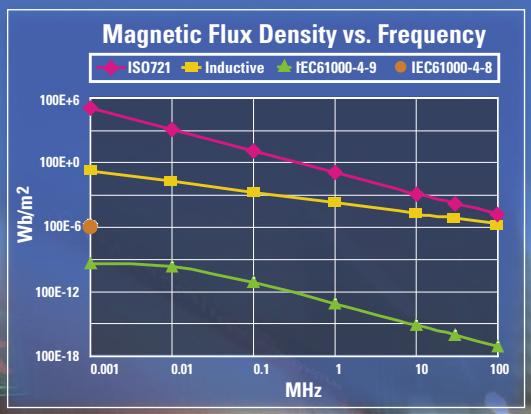


Figure 1 Increasingly, analog blocks depend on tight interaction with digital blocks and even processors, requiring a sophisticated mixed-mode simulation environment even for behavioral modeling (courtesy Analog Devices Inc).

Total Noise Immunity

High Speed, Reliable Capacitive Isolation

TI's capacitive digital isolation technology conveys data across an oxide barrier at significantly higher rates than optocouplers, has substantially improved common mode transient immunity and greatly reduced power requirements. The ISO721 – a highly reliable, single component, EMI resistant solution ideal for your data transmission needs.



High Performance. Analog. Texas Instruments.

For a datasheet, sample and evaluation module, visit
www.ti.com/iso721

Technology for Innovators™

Texas Instruments

power gating and dynamic voltage and frequency scaling. The use of these techniques means that the clock and supply networks on an SOC can change their effective topology, as well as their frequencies and voltages, on the fly, enormously complicating analysis. Ideally, no paths would exist between the supply pins on analog and digital blocks. But, with the increasing use of digital feedback and control into analog blocks and with the inevitable parasitic coupling of large transients across nets, you cannot assume that analog clock, power, and ground signals are clean. Many teams now perform detailed extractions of these nets and use Spice to model them before tape-out.

Perhaps more problematic still in SOCs with high-speed digital blocks, noise can couple into any node in an analog circuit through the substrate. This problem is especially worrisome for a number of reasons. First, the designer may not understand the location of the noise sources even after performing detailed floorplanning. The bad news may not arrive until the designer completes detailed placement. Second, digital designers are usually unaware of the noise their circuits are injecting into the substrate, so they may be no help in identifying signal sources, let alone locating or quantifying them. Digital designers don't tend to think in terms of digital signals having frequency spectra. Third, neither design teams nor, frankly, foundries are likely to have adequate substrate-electrical models unless they have been previously involved in RF design. Fourth, in advanced processes, the high-frequency components of digital transients—and even harmonics from digital clocks—are so far into the RF region that simple substrate models may be highly misleading. So, even if the designers could locate and accurately model the noise sources, it might be anyone's guess what effect the sources would have on a particular node.

More widely known coupling problems between chunks of metal in the interconnect stack are just as problematic. Some design disasters on processes as large as 180 nm forced digital designers to recognize the role that capacitive coupling could play in signal integrity. But the tools that designers built to deal with the problem in the digital domain generally use static guidelines to screen layouts for possible capacitive coupling. The tools then either just flag those problems or degrade the delay parameters on the net on the assumption that, because everything is synchronous to the same clock, if another signal is coupling onto a victim net, you just have to wait for the aggressor to settle and the noise will go away.

This model is less than helpful for analog blocks, of course. Some low-performance analog blocks hold during clock transitions of surrounding digital circuitry or simply shut down while big digital clock trees are operating. But, most of the time this approach is impractical, and the designer must protect the continuous-time analog circuits from aggressors. No tools in the digital domain can examine the surroundings of an analog block with that level of detail. So, it again comes back to the analog-block integrator: Extract accurate models of the parasitic capacitances, add them into the Spice model, and perform detailed simulations.

THE INDUCTANCE NIGHTMARE

This approach is not fun, but it is manageable. Another problem looming on the horizon—inductive coupling—is less manageable, however. A couple of years ago, researchers in digital tools were concerned that inductive coupling would finally defy Moore's Law, because inductive coupling gets more efficient with increasing frequency, and it strongly depends on the 3-D geometry of the aggressor and victim structures. Worse, the victims need not be nearby. All these issues appeared to present an uncomputable problem. Subsequent evidence

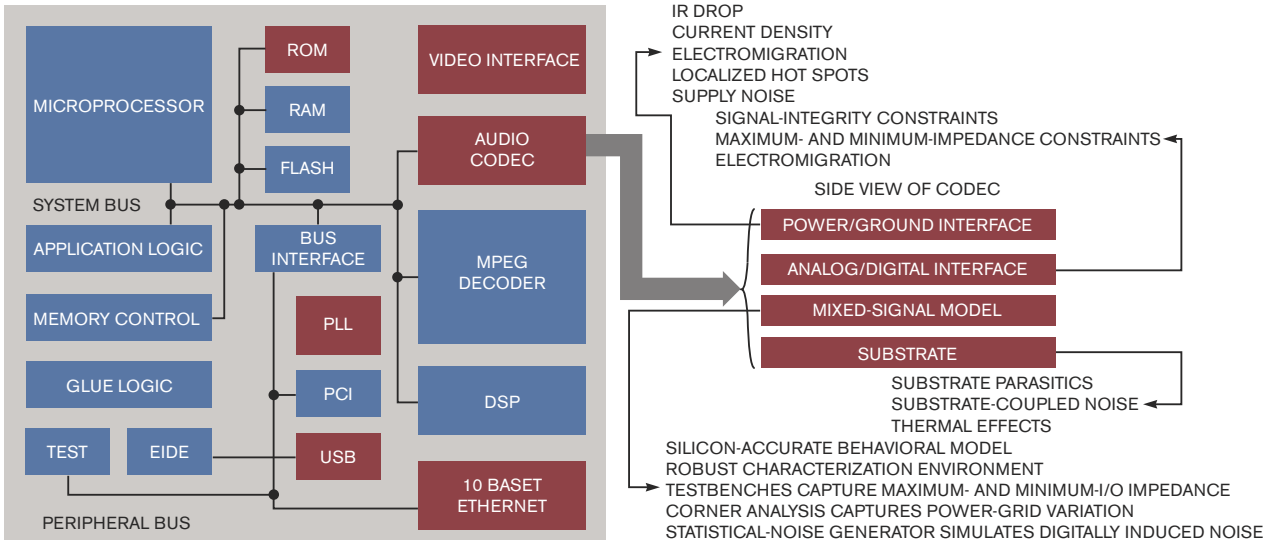


Figure 2 At every level of abstraction, a precision analog block breaks the simplifying assumptions on which digital-IP reuse depends. This approach complicates block integration (courtesy Cadence Design Systems).

A function generator set for action

The Agilent 33220A packs in bench and test-system features

Agilent 33220A 20 MHz function/arbitrary waveform generator

- *Low-distortion basic waveforms*
- *Variable edge-time pulses up to 5 MHz*
- *Arbitrary waveforms up to 64K points*
- *AM, FM, PM, FSK, and PWM modulation*
- *Sweep and burst operation modes*
- *Open connectivity via USB, LAN, and GPIB*

Agilent Open

Agilent Direct

Get the application note,
8 Hints for Getting More from Your Function Generator
www.agilent.com/find/8-hints

Or call a Live Sales Engineer now if you are ready for a new High Performance Function Generator
u.s. 1-800-829-4444 Ext. 5463
canada 1-877-894-4414 Ext. 5463

The Agilent 33220A function generator packs outstanding performance into a very compact design.

Able to fit into your rack or on your bench, the 33220A is loaded with multiple signal powers—from stable, accurate output of low-distortion sine waves to variable edge-time pulses and custom arbitrary waveforms.

Front panel operation provides the ease of use you'd design yourself—because Agilent created the 33220A in consultation with customers like you. You'll find access to all major functions and adjustments at your fingertips. Agilent Open capabilities mean system readiness, compatibility with popular software environments, plus built-in USB, LAN, and GPIB ports.

The Agilent 33220A is powerful and affordable enough for uses from R&D to manufacturing. Its software compatibility with the widely used 33120A and 33250A function generators ensures easy integration into new or existing systems. To enhance your function generator power now, get tips at www.agilent.com/find/8-hints.

Agilent Technologies

suggests that, even for multigigahertz designs, the problem for digital SOCs may be much less than designers originally feared. However, no such reason for reassurance exists about the interaction between high-speed digital circuits and—in particular—analog RF blocks with on-chip inductors. Designers must consider inductive coupling for blocks operating at these frequencies.

Even connecting the signal pins to those of surrounding blocks involves a different skill for analog blocks from that for digital blocks. In the digital world, the only problem is to connect the right components with a trace that routes. If loading issues exist, the timing-analysis tools and buffers will handle them. In the analog world, every input and output requires more thorough specification (**Figure 3**). Voltage levels are not approximate and understood; engineers must specify them. Signal spectra are important. Noise that couples into the block from inputs or through outputs is important. Impedances matter. You could insert an analog block into a design, connect its pins in a logically correct manner, and inadvertently subject the block to impedances that prevent its operation. So, the noise and impedance characteristics of the pins on other blocks, as well as the impedances of the interconnect lines themselves, become issues.

The situation becomes even more interesting in designs using 130-nm or smaller geometries, in which design-for-manufacturing tools may change the physical layout of a metal layer after routing is complete. Tools that move metal lines to comply with line-pitch or -density rules can substantially change the electrical characteristics of a metal run. Tools that insert "dummy" metal—islands of metal that do not physically connect to the rest of the circuit, but keep the density of metal features constant across the surface of a layer—can also change the metal run's electrical characteristics. Dummy metal beside or over an analog path can provide a new set of parasitic capacitors to many other circuit nodes.

GETTING IT DONE

All of these problems may sound formidable. Yet engineers say that solving them is difficult but not impossible. It's worth examining how a few shops are dealing with these issues to see what the future might be for analog integration into SOCs for the rest of us. One strategy is to encapsulate the analog IP in a purely digital wrapper. This technique allows you to model the block at the system level as a digital block and to treat it as conventional hard IP during physical design. This approach requires that the entire analog content of the design fit into one block or at least that the analog blocks have only digital links to each other. It also requires that you put enough thought into the isolation requirements and that you can integrate the block using a set of guidelines that eliminate any possibility of injected noise's becoming a factor in the performance of the circuitry. That requirement in turn means using conservative design techniques. "The concept of analog building blocks is viable, but it implies higher power, greater area, and lower performance," says Wolfgang Meier, senior manager of business development at Infineon Technologies' ASIC operation.

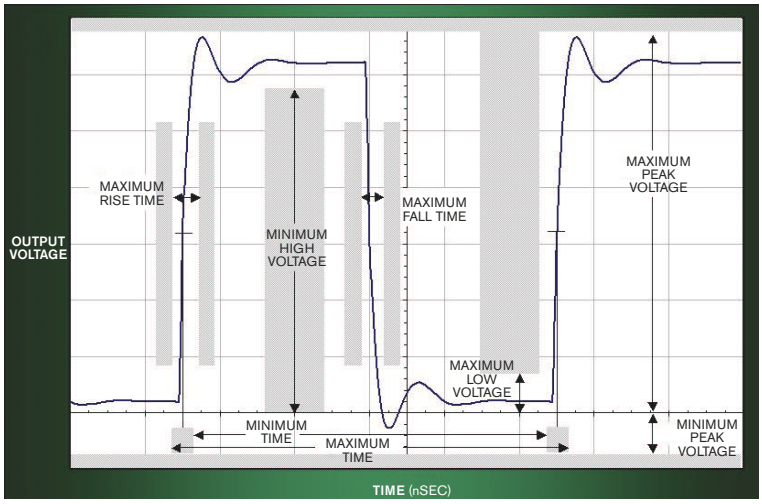


Figure 3 Just writing the specifications for an input to an analog block can become a significant design undertaking, requiring detailed knowledge of the internal circuitry (courtesy AMI Semiconductor).

Such conditions may not be entirely practical in the ASIC world, but they can exist in another important technology: microcontrollers. Here, analog performance may not be a differentiating factor, and long experience with a single analog library may refine the integration process until it works smoothly. This scenario has been true at Silicon Laboratories. "The tradition was 100% hand-routing for analog," says Silicon Labs' vice president of technology, Douglas Holberg. "But our principle has been to exploit reuse. Today, we can effectively reuse 8- and even 16-bit data-converter blocks with a drop-in model. The integrator has to understand the block through the interface stages, and he has to understand the top-level process for assembling blocks in our methodology—practices about how you take a signal across a power-supply boundary or between clock zones, for instance. And we use techniques, such as deep N-wells, to make the block look as digital as possible."

But is the result turnkey reuse? "In the beginning, it worked only because we had the analog experts involved to keep the integrators from breaking the block,"

FOR MORE INFORMATION

Actel
www.actel.com

AMI Semiconductor Inc
www.amis.com

Analog Devices
www.analog.com

Barcelona Design
www.barcelonadesign.com

Cadence
www.cadence.com

Infineon Technologies
www.infineon.com

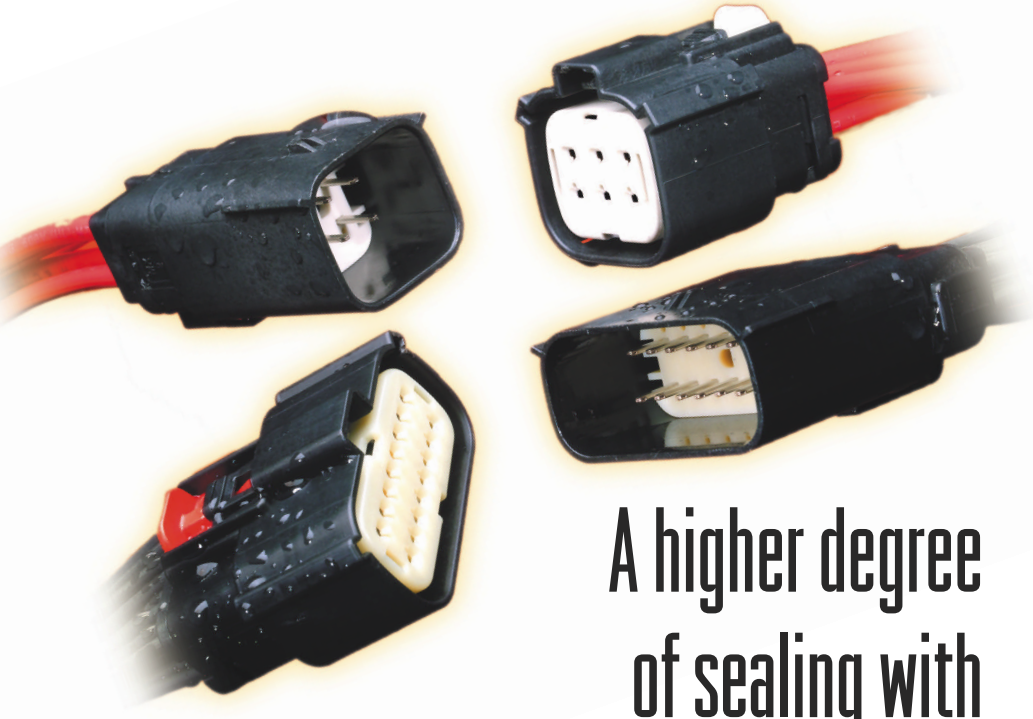
Knowlent
www.knowlent.com

Silicon Laboratories
www.silabs.com

Wolfson Microelectronics
www.wolfson.co/uk

ZMD
www.zmd.com

The MX150™ family represents the highs and lows of interconnection:



A higher degree of sealing with lower applied costs

The pre-assembled MX150/150L connector system offers rugged sealability and affordability.

That's right, the pre-assembled MX150 product line includes seals, housings and terminal position assurance (TPA) in one connector. This means you simply crimp, poke and plug your way to a fully protected, environmentally-sealed connector.

Suitable for a wide wire range of signal and power applications, the MX150 family was designed specifically to take on harsh and wet conditions – such as those found in RVs, off-road construction vehicles, agricultural equipment, industrial machinery, outdoor lighting, boats, and other tough industrial and commercial environments. This product meets IEC IP67 requirements, complies with UL/USCAR-2 standards and offers UL and SAE wire compatibility.

In addition, Molex is your single source for just about every kind of innovative industrial connector technology. And, if need be, we can work with you to design a custom solution that meets your precise specifications.

When it comes to high performance interconnects and integrated subsystems for harsh environments, we've got your solution all sealed up.

Industrial Division Headquarters
Pinellas Park, FL U.S.A.
Tel: 800-800-0449

Far East North Headquarters
Yamato, Japan
Tel: 81-462-65-2324
feninfo@molex.com

Far East South Headquarters
Jurong, Singapore
Tel: 65-6-268-6868
fesinfo@molex.com

European Headquarters
Munich, Germany
Tel: 49-89-413092-0
eurinfo@molex.com

Corporate Headquarters
2222 Wellington Court
Lisle, Illinois 60532 U.S.A.
Tel: 630-969-4550
Fax: 630-969-1352

molex®

Bringing People & Technology Together, Worldwide℠

www.molex.com/ind/mx150.html

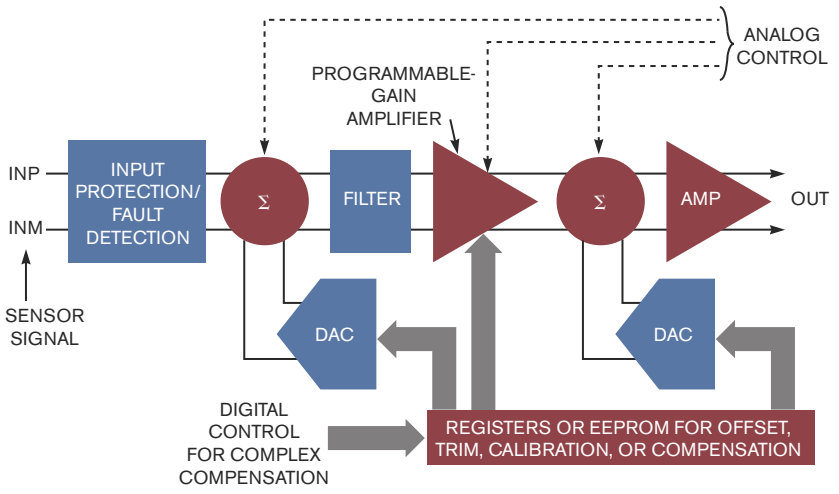


Figure 4 As transistors get smaller and analog-signal processing gets more complex, digital circuits must assist in trimming, compensating, and sometimes enhancing the functions of analog-signal paths (courtesy AMI Semiconductor).

Holberg says. Such a technique may result in turnkey reuse now, however.

AN ASIC APPROACH

What happens when you can't detune the analog blocks to improve integration? In that case, the model often becomes one of heavily assisted ASIC design. In a conventional digital-ASIC relationship, the customer would hand off a verified netlist, and the ASIC house would do the physical design and extraction. Similarly, in a mixed-signal ASIC, the customer may obtain relatively simply functional models of analog blocks from the ASIC vendor's library. The customer would use mixed-signal-simulation tools to approve the behavior of the blocks, and then the vendor design team—strong in analog-design skills—would integrate the analog functions into the design.

This model is the one that AMI Semiconductor uses, for example. The company keeps an extensive library of analog functional blocks and provides models to customers. When the customer is happy with the netlist, including the analog functions, the AMI team takes over and does the integration. That process may not involve an exact drop-in assembly. "We can leverage an extensive analog-block library," explains AMI's director of mixed-signal products, Ryan Cameron. "So, we rarely have to start with a clean sheet of paper. But the result is rarely a drop-in, either. Except for simple blocks, it's probable that the analog circuitry will receive modification in some way during the integration process." That situation means that senior analog designers must take part in the process.

AMI tries to use a multitrack design flow, in which behavioral-modeling engineers work with customers to establish architecture and block specifications that they base on chip-level simulations. They must also define waveforms, envelopes, and corner-case behaviors for the analog pins. Meanwhile, circuit designers pull blocks from the library and tweak them to fit the chip-level specifications. Ideally, the two meet in the middle; designers then adjust the blocks to the needs of the chip design and adjust the chip architecture to require a minimum of new analog design. Two areas that most frequently become issues in adapting a block, according to Cameron, are initialization sequences—especially for high-voltage blocks—and details in the board-level environment.

Designers from another quarter equally emphasize the importance of communication between chip- and circuit-level designers during integration. Actel Corp acquired much of the analog IP it integrated into its family of mixed-signal FPGAs. That acquisition required a significant effort on Actel's part to assemble the analog blocks into a chip along with

E-T-A Circuit Breakers
Thermal
Thermal Magnetic
Magnetic
High Performance
Electronic

No two circuit breaker applications are alike

Only E-T-A offers more technologies

Many circuit protection applications appear the same but every application is different requiring a specific circuit protection solution. Only E-T-A provides the most complete range of available circuit protection technologies.

More technologies allow for superior, more precise circuit protection. It is critical that your design is protected with the correct circuit protection. Your reputation depends on it.

One call to E-T-A will ensure your design has the right circuit protection technology to enhance your products safety, reliability and brand reputation.

Go to www.e-t-a.com/ipod4 for your chance to win one of 10 video iPods®

3120-F7
Applications include: marine, medical and office equipment, appliances and tools.

E-T-A®
Circuit Protection & Control

WWW.E-T-A.COM
1-800-462-9979

You need this clock generator

CG635 – Precise, low jitter clocks from DC to 2.05 GHz

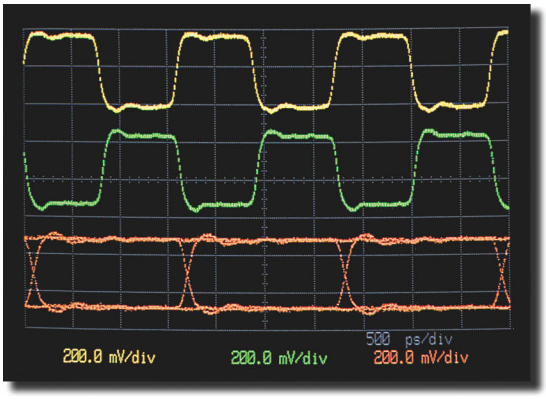
- **Square wave clocks from DC to 2.05 GHz**
- **Random jitter <1 ps (rms)**
- **80 ps rise and fall times**
- **16-digit frequency resolution**
- **CMOS, LVDS, ECL, PECL, RS-485**
- **Phase adjustment and time modulation**

The CG635 Synthesized Clock Generator provides square wave clocks between DC and 2.05 GHz that are clean, fast and accurate. With jitter less than 1 ps, transition times of 80 ps, and 16 digits of frequency resolution, the CG635 will meet your most critical clock requirements.

The instrument can provide clocks at virtually any logic level via coax or twisted pairs. The outputs have less jitter than any pulse generator you can buy, with phase noise that rivals RF synthesizers costing ten times more.

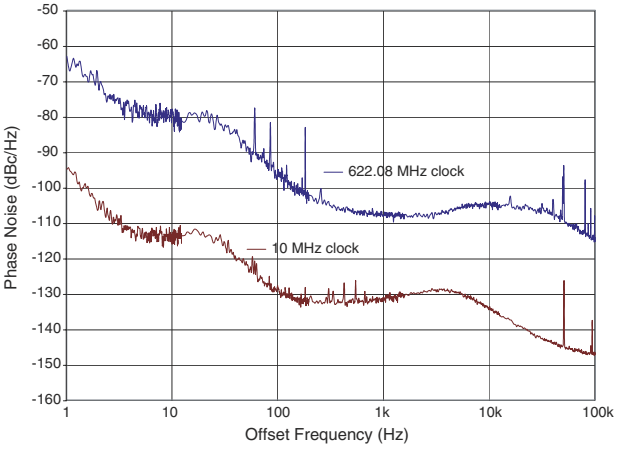
Optional OCXO and rubidium timebases improve frequency stability by 100× and 10,000× over the standard crystal timebase. And an optional PRBS helps you evaluate high-speed serial data paths.

Whether you are trying to lower the noise floor of an ADC, increase SFDR of a fast DAC, or squash the bit error rate in a SerDes, the CG635 is the tool you need to get the job done.

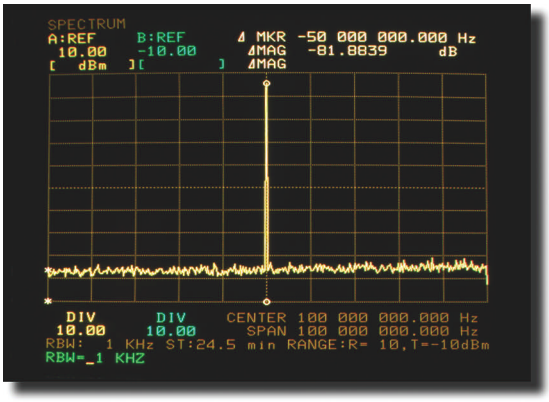


Clock and PRBS signals at 622.08 MHz

Plot shows complementary clock and PRBS (opt. 1) outputs at 622.08 Mb/s with LVDS levels. Traces have transition times of 80 ps and jitter less than 1 ps (rms).



Phase noise for 10 MHz and 622.08 MHz outputs



RF Spectrum of a 100 MHz clock

Graph shows a 100 MHz span around a 100 MHz clock. Only two features are present: the clock at 100 MHz, and the spectrum analyzer's noise floor (around –82 dBc).

SRS Stanford Research Systems, Inc.

Phone: (408)744-9040
www.thinkSRS.com

the flash-based logic array and I/O circuitry, keeping the blocks configurable and not breaking them.

A POSSIBLE FUTURE

So, does a block-assembly methodology for mixed-signal SOCs depend on having a staff of analog gurus in the back room? Today, the answer is probably "yes." But some changes on the horizon might make a difference. One is the increasing power of mixed-signal-design environments. As it becomes increasingly possible to accurately characterize analog blocks—including sensitivity analysis, not just functions and parameters—with a few test chips, it becomes more possible to harden analog blocks for the misfortunes that can happen during integration. It also becomes possible to characterize and simulate more of the important interactions between the block and its neighbors—moving this analysis from the Spice domain and into the realm of faster and less user-intensive mixed-signal-simulation tools. But tools for sign-off-quality noise modeling and analysis are still problematic. "It's an area in which we still have some work to do," admits a marketing director at one EDA vendor. "The work is going on only at the university level today."

Another important change is also under way: the increasing degree to which analog circuits are coming under digital control. Engineers at Actel, for instance, compensate the on-chip RC oscillators in the company's devices for voltage and temperature using a table in flash memory. AMI often puts a fair amount of digital programmability into analog blocks early in the design process and then backs much of it out as the device heads from early silicon to full production (**Figure 4**). In that way, AMI can use nonvolatile memory to trim early devices to meet specifications, and, as the company gains a better understanding of the design, it can pull out the trimming circuitry to improve die area.

This trimming capability may be as simple as controlling MOSFET switches in a resistor or capacitor network. It may be large-scale yet delicate, such as switching in and out stages in an RF-power amplifier, as ZMD does in the linear power amplifier on its single-chip ZigBee sensor-interface devices. Or it may mean actually driving a DAC from the digital trimming signal to bias a node.

Today, such techniques find use primarily in early silicon versions and test chips, as at AMI, or in inherently messy analog problems, such as 90-nm RF amplifiers in single-chip cellular handsets. But engineers could conceivably use these trimming techniques as aids to integration. By identifying the points in an analog block that prove most sensitive to changes in the external environment and making them digitally tunable, designers could make trade-offs of performance, power, and noise immunity after the integration process or even after manufacturing. This approach would allow a relatively naïve design team to drop in a configurable analog block, perform tape-out, and then experiment with the configuration bits on the engineering samples to get the block working. This inelegant approach might extend the range of blocks that designers can use in block assembly. Such tactics may be necessary in any case simply because of the process variations at geometries smaller than 130 nm.

So, analog blocks can be black boxes in SOC design only if they are simple or if your ASIC vendor has a back room full of analog designers. In the future, however, things may change dramatically. EDN

MORE AT EDN.COM

- We encourage your comments! Go to www.edn.com/060511cs and click on Feedback Loop to post a comment on this article.
- To see how little has changed in two years, read an article from 2004 at www.edn.com/article/CA409045.
- To read more about ZMD's ZigBee project, try www.edn.com/article/CA6325290.

NAND Flash

Toshiba MLC NAND leadership provides the power to launch today's applications.

It takes power to launch a successful product in this world of technology migration and converging applications. So you need the power of a proven, leading-edge memory solution from an industry leader. That's MLC NAND Flash from Toshiba. • With its high density and proven reliability, our MLC NAND Flash is enabling today's new applications while answering the cost/performance challenges of many consumer designs. For your high-density storage needs, Toshiba MLC NAND Flash can help you deliver the right solution. • Visit us at **mlcnand.toshiba.com** and find out how the industry leadership and design experience offered by Toshiba can give your next consumer design its best shot at success.

mlcnand.toshiba.com

INNOVATOR OF FLASH MEMORY

ISO 9001:2000 CERTIFIED

TOSHIBA

BY BRYAN KANTACK • AGILENT TECHNOLOGIES

Spread-spectrum clocking: measuring accuracy and depth

DESIGNERS USE DATA-RATE SMEARING TO SPREAD EMI ACROSS MULTIPLE FREQUENCY BANDS. LEARN HOW TO QUICKLY TEST AND VERIFY YOUR IMPLEMENTATION.

Many of today's high-speed serial designs use embedded clocks to avoid routing and timing issues involved with separate data and clock signals and to free up precious real estate on board designs. These embedded clocks are not separate clock signals coupled to the original data signal. Instead, the clock times the data-transmitter output, and a separate PLL recovers the clock signal from the data at the receiver. Because the data is a synchronous source of electrical energy, the clock frequency of the data focuses at half the data rate and other transition-period harmonics and creates EMI (electromagnetic interference) at those frequencies. EMC (electromagnetic-compatibility) labs use broad-spectrum analyzers to measure the EMI of a device in discrete bands—120 kHz wide, for example—when determining compliance.

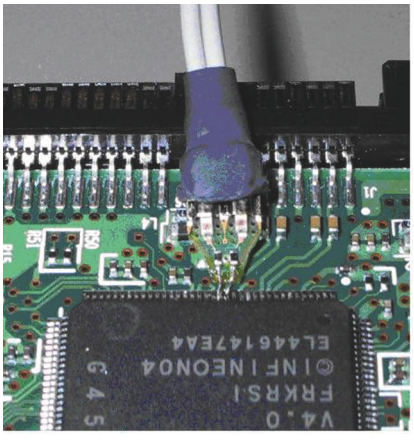


Figure 1 A differential active probe with 13-GHz bandwidth connects to the transmitter-package pins on a high-speed serial link.

Many device vendors have now turned to SSC (spread-spectrum clocking), a method of data-rate smearing, to avoid having too much EMI within any one band when an EMC tester tests the equipment. SSC further helps to reduce crosstalk between adjacent asynchronous buses in complex systems, such as PCs or servers, in which many high-speed serial peripheral buses operate simultaneously. You implement spread-spectrum clocking by frequency-modulating the data-transmission output of a transmitter to spread the spectral-energy peaks out over a wider bandwidth. The total energy on the bus, therefore, does not decrease but spreads over a wider frequency band. A PLL at the receiver then uses a closed-loop highpass-filter function to track the frequency modulation of the SSC and recover the data. You need to measure your SSC's implementation accuracy using a high-speed real-time oscilloscope with clock-recovery capability and a measurement-trending software package.

CONNECT TO THE TRANSMITTER

It is important to consider the methods available to get a multigigabit signal from a design without disrupting the signal's voltage and timing characteristics. Many designers allot enough space to load SMA connectors onto their development boards to directly measure the transmitted signal using an oscilloscope. This practice is usually a good one to use early in chip-set validation, but it may be impossible once the board goes to final layout for production prototyping. At this stage, it is crucial to have robust, high-performance test tools available to debug your target system and allow for precision measurements at either the transmitter or the receiver end of a high-speed serial link. Today's state-of-the-art differential active voltage probes now offer as much as 13 GHz of measurement bandwidth with less than 0.22 pF of capacitive loading at the probe tip. These tools typically employ small, passive test circuits with miniature connectivity to the device under test and an active amplifier to transmit the signal with minimal distortion back to an oscilloscope for viewing.

Figure 1 illustrates a small, 13-GHz differential active voltage probe that connects directly to the package pins of a high-speed, differential transmitter on an active link. You should use the highest bandwidth probing tool available to avoid inducing unwanted slew-rate limitations or artificial signal anomalies into the signal under test. Some high-speed serial-link standards additionally specify compliance-test points, which typically appear at a common connector interface in which the high-speed serial transmitter pair mates with the corresponding receiver pair of a similar device to which it connects. An example would be the SATA (Serial ATA) electrical-compliance interface, which measures the electrical characteristics

of the transmitter at the SATA connector, because it connects to a high-quality laboratory load. A high-bandwidth oscilloscope and reference-quality test connector provide the high-quality load. The equipment has greater than 20 dB of return loss at 5 GHz and 10 dB of return loss at 8 GHz. **Figure 2** illustrates this type of laboratory load for SATA electrical-performance validation and compliance testing.

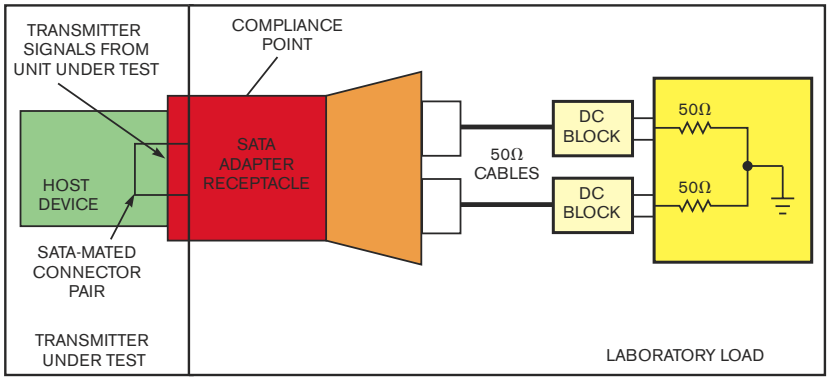


Figure 2 In a SATA (Serial ATA) laboratory load for 3-Gbps SATA-transmitter-compliance testing, the equipment has greater than 20 dB of return loss at 5 GHz and 10 dB of return loss at 8 GHz.

Once you have established an appropriate connectivity method to properly terminate and capture the signal under test, you can measure the SSC modulation depth and frequency. You should use a repeating "1010" data pattern to test the SSC's performance, and you should send the repeating data pattern at the highest supported data rate for the bus. This approach ensures that the spectral content of the digital signal focuses primarily at one-half the data rate and reduces the effects of data-dependent jitter in the measured data rate. You should also select an oscilloscope with at least enough bandwidth to capture the fifth harmonic of the nominal data rate and enough sample rate to avoid aliasing on a single-shot data capture. For 3-Gbps SATA, this requirement would involve an oscilloscope bandwidth of no less than 7.5 GHz and at least 20G samples/sec of single-shot sample rate. The SATA electrical specification recommends 10 GHz of bandwidth, and a common rule for digitizing oscilloscopes is that the minimum sample rate should be 2.5 times the oscilloscope bandwidth to avoid aliasing of frequencies near the oscilloscope's upper bandwidth limit. Several real-time oscilloscopes are now available that meet the 10-GHz and 25G-sample/sec minimum requirements to most accurately measure the SSC profile of 3-Gbps data streams.

CONFIGURING THE MEASUREMENT

You can easily measure the accuracy of SSC using a real-time oscilloscope with deep memory and a jitter-measurement package that can recover a clock and can trend the measured time gaps between the transitions in a fast serial data stream. You must first evaluate the repeating frequency of your SSC modulation and find a digitizing, real-time oscilloscope with enough memory to capture at least one full period of the SSC's modulation frequency at its maximum sample rate, which is 40G samples/sec on today's highest bandwidth real-time oscilloscopes. For example, if you have a 33-kHz frequency modulation on a 3-Gbps data rate, then you will need approximately 2 million points of memory at 40G samples/sec (2 million samples×25 psec/sample=50 µsec) to capture the 30.3-µsec modulation period of the SSC. **Figure 3** shows a 33-kHz, triangular SSC modulating a 3-Gbps data signal. The triangular SSC profile downconverts the data signal's frequency from 0 to −0.5% to reduce the concentration of EMI at any one frequency. This action limits the data rate to 2.985 to 3 Gbps, translating to a change of 0 to −15 MHz from the nominal line rate.

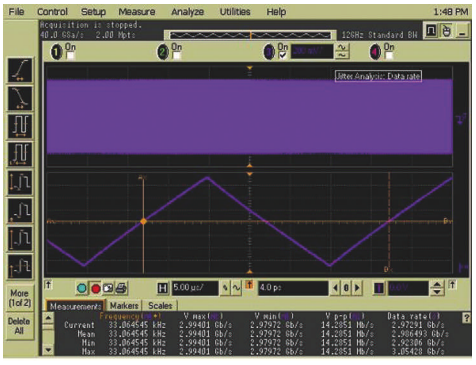


Figure 3 A 33-kHz, triangular spread-spectrum clock downspreads the 3-Gbps data signal's frequency from 0 to −0.5% to reduce the concentration of EMI at any one frequency.

This 13-GHz, real-time oscilloscope includes the EZJIT measurement-trending and jitter-analysis software, which allows designers to observe the change in the data rate of the data that this link is transmitting, as well as the frequency accuracy of the 33-kHz, triangular-SSC profile that is frequency-modulating the data. A simple trend measurement of the data rate shows all variations in the data rate due to both the SSC-frequency modulation and as short-term variations in the data rate, which can make it difficult to accurately measure the SSC profile. Therefore, most high-speed-serial-bus specifications that allow transmitters to use SSC specify a narrower frequency range over which to measure the SSC's modulation depth and frequency accuracy. The SATA electrical specification specifies a lowpass filter that you must apply to the measurement trend with a cutoff frequency of 60 times the maximum frequency, or approximately 1.98 MHz, for the triangular SSC.

The real-time oscilloscope offers a smoothing feature in its measurement-trending-software package that acts as a lowpass filter for removing higher frequency variations in the data-rate trend. Sources of data-dependent, random, or bounded uncorrelated jitter above the desired 1.98-MHz cutoff frequency cause these variations. As a general guideline, a 3-Gbps SATA link using a 1010, or high-frequency-data, pattern and having a desired cutoff frequency of 1.98 MHz would require 335 smoothing points.

MODULATION AND FREQUENCY

Because the measurement trend plots the data rate on the vertical axis versus time on the horizontal axis, you

REDUCE DEVELOPMENT COST!

TALK TO US

800-496-5570

REDUCE *your power development cost by specifying Vicor modular DC-DC converters. We offer the widest range of standard input voltages, output voltages, and power levels in the industry. They all come with complete safety agency approvals, and Vicor's high power densities allow more flexible packaging. A full range of online design tools and access to our worldwide applications engineering staff help ensure that you achieve the most cost-effective power design.*

TALK TO US*, and claim your Multimeter. You'll find out how you can reap the benefits of designing with Vicor high-density DC-DC converters. Faster time to market, greater power density and performance, and higher reliability are always affordable. Call 800-496-5570 or go to* ***vicorpower.com/edn2*** *for more information.*

Always Affordable!

vicorpower VICOR com

can use the oscilloscope's automated amplitude measurements to measure the minimum and maximum line-speed rates over an entire cycle of the SSC-modulation period, which in this case is nominally 30.3 µsec. Additionally, you can apply the oscilloscope's automated frequency measurement to the data-rate-measurement trend and adjust its thresholds to measure the frequency at the 50% threshold of the rising or falling edges of the filtered triangular-SSC profile. **Figure 3** illustrates several automated oscilloscope measurements that quickly and accurately identify the maximum and minimum data rates of the measured data, which the triangular-SSC profile modulates, as well as the repeating frequency of the SSC profile. The oscilloscope's markers automatically track the frequency measurement, but they can also track the maximum and minimum data-rate measurements. Automated oscilloscope measurements provide a significantly more accurate assessment of the SSC's modulation depth and frequency than traditional methods of manually adjusting data markers.

Correctly setting up and measuring SSC's profile-modulation depth and frequency accuracy is simple with today's state-of-the-art, high-performance oscilloscopes and automated measurement-trending software. You must carefully choose your connection to the transmitter and the appropriate bandwidth and sample rate of the measuring oscilloscope to ensure the integrity of the data signal and the proper reference test load. You must also apply an appropriate lowpass filter to remove higher-frequency-modulation domain "noise" from the measurement trend, exposing only the signal characteristics of interest on the SSC profile you're measuring. In addition, automated amplitude and frequency measurements from the oscilloscope's measurement menu provide simple and accurate measurements of maximum and minimum data rates and SSC-profile frequency, saving you valuable time. EDN

MORE AT EDN.COM

Go to www.edn.com/ms4184 and click on Feedback Loop to post a comment on this article.

AUTHOR'S BIOGRAPHY

Bryan Kantack is a serial-storage-product manager at Agilent's high-performance-oscilloscope division, where he has worked for five years. He currently focuses on new-product development for enterprise- and network-storage physical-layer testing. Kantack has a bachelor's degree in electrical engineering from Kansas State University (Manhattan, KS) and a master's degree in finance from the University of Colorado (Colorado Springs). In his spare time, he enjoys running, mountain biking, and spending time with family and friends.

Low Voltage Hot Swap Control

High Performance Analog Solutions from Linear Technology

High availability systems must operate continuously without interruptions in service. To achieve this level of reliability in large systems with many circuit cards, you must be able to add new cards and replace obsolete or damaged cards without powering down the system. While most power is distributed at higher voltages to minimize current and to reduce the effects of voltage drops, many applications require low voltages to be delivered.

Low Voltage Hot Swap Solutions

Most high current Hot Swap™ controllers utilize external, low $R_{DS\ (ON)}$ MOSFET switches and accurate current sense resistors to control current. The current sense resistor, combined with the comparator, form an electronic circuit breaker that turns off the switch if the load current exceeds a set limit. The threshold of this comparator, V_{CB}, determines the voltage drop across the sense resistor in addition to the drop across the switch. For sub-3V systems, this represents a significant portion of the total supply voltage.

Many systems experience short duration transients that are part of normal operation. For example, systems require large, short duration currents when writing a block of data to memory. These events may cause the load current to exceed the circuit breaker threshold momentarily and falsely shut off the switch. A second level of control circuitry distinguishes between real faults and operating transients and provides appropriate fault protection. A fast amplifier actively limits current to solve this issue.

Several Hot Swap controllers from Linear Technology, shown in Table 1, include features optimized for low voltage applications such as 1V microprocessor core voltages, where a 3.3V bias supply may also be available. Compared to 50mV circuit breaker thresholds, a low V_{CB} of 25mV and the ability to work properly with common mode voltages approaching ground minimize the drop in the power path.

Table 1. Low Voltage, Low V_{CB} Hot Swap Controllers

Parameters	LTC®4216	LTC4213	LTC4221	LTC4215
Circuit Breaker Threshold	25mV	25mV, 50mV or 100mV (selectable), MOSFET V_{DS} Sensing (No R_{SENSE})	25mV	25mV
Circuit Breaker Voltage Range	0V to 6V	0V to 6V	1V to 13.5V	2.9V to 15V
Bias Supply Required	2.3V to 6V (for circuit breaker operation below 2.3V)	2.3V to 6V (for circuit breaker operation below 2.3V)	V_{CC1}, 2.7V to 13.5V V_{CC2}, 1V to 13.5V $V_{CC1} \geq V_{CC2}$	N/A
Package	4mm x 3mm 12-lead DFN, 10-lead MSOP	3mm x 2mm 8-lead DFN	16-lead SSOP	5mm x 4mm 24-lead QFN, 16-lead SSOP
Additional Features	Dual-level overcurrent protection, adjustable soft-start, adjustable overcurrent response time	Dual-level overcurrent protection	Configurable supply sequencing, dual-level overcurrent protection, foldback current limiting, adjustable soft-start	8-bit ADC for current and voltage monitoring, I²C Interface, dI/dt soft-start, foldback current limiting

LINEAR TECHNOLOGY

Low Voltage Hot Swap Control

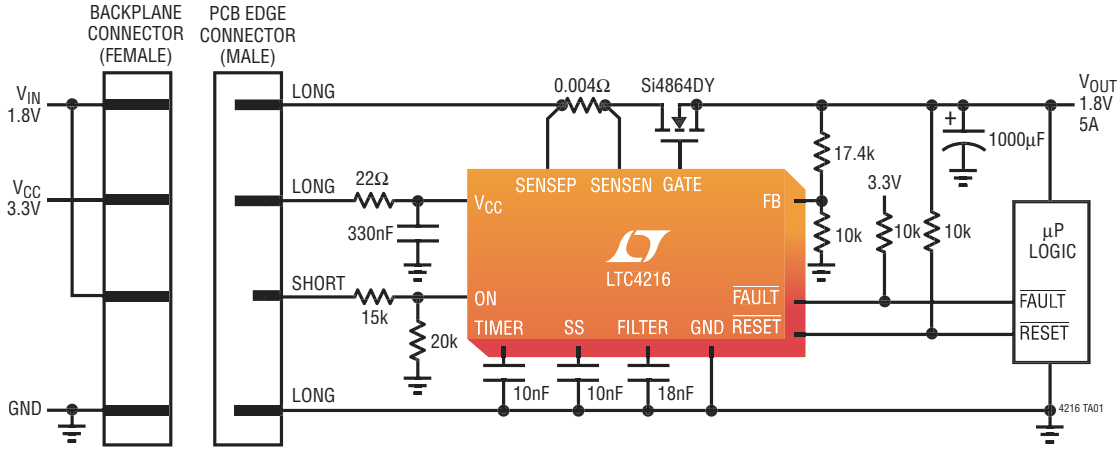


Figure 1. Hot Swap Control for 1.8V Core Supply

Ultra Low Voltage Hot Swap Controller

The LTC4216 is an ultralow voltage Hot Swap controller that protects load voltages ranging from 0V to 6V (see Figure 1). In order to meet demands for faster and more efficient data processing, modern microprocessor systems are designed with lower voltage implementations. The LTC4216 answers the inrush control needs of such systems and allows for the safe insertion and removal of boards from a live backplane. Together with an analog current limit amplifier, an electronic circuit breaker with adjustable response time provides dual level overcurrent protection. The IC also features an adjustable soft-start circuit to limit the rate of change of the inrush current at startup.

The LTC4216 is offered in 10-lead MSOP and 4mm x 3mm 12-lead DFN packages, and is an attractive solution for today's servers, telecom equipment and base stations, whose low voltage design is driven by the increasing complexity and operating speeds of low power microprocessors.

No R_{SENSE} Electronic Circuit Breaker

For even lower series voltage drop, the LTC4213 electronic circuit breaker senses load currents with the $R_{DS(ON)}$ of an external MOSFET and eliminates the need for a sense resistor. This method not only reduces voltage and power loss in the switch path, but also lowers the cost and simplifies design. This is especially beneficial to low voltage systems since the sense resistor voltage drop constitutes a significant portion of the supply voltage. For ultralow voltage applications, the LTC4213 operates over a bias supply range of 2.3V to 6V and monitors voltages from ground up to 6V (see Figure 2). As with the LTC4216 above, the bias supply allows continuous circuit breaker operation all the way down to 0V.

The electronic circuit breaker offers three pin-selectable V_{DS} thresholds of 25mV, 50mV and 100mV. The select pin can be stepped dynamically,

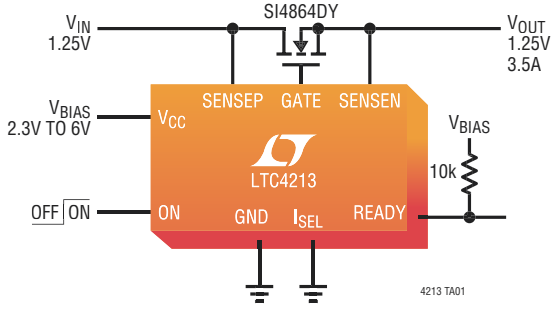


Figure 2. Electronic Circuit Breaker Requires No Sense Resistor

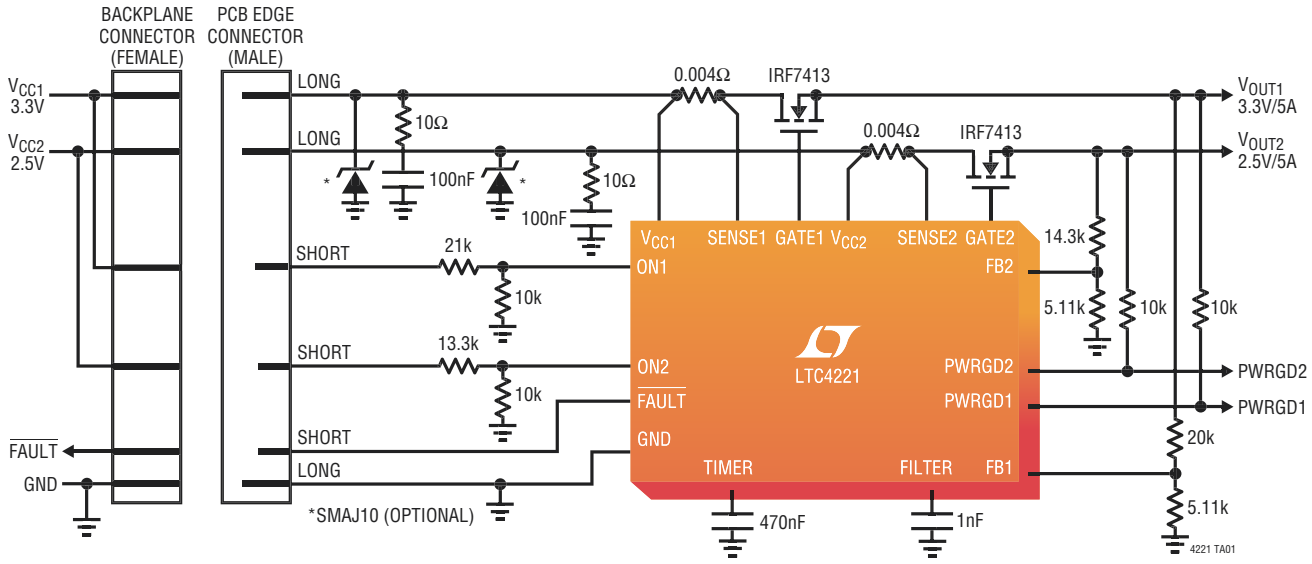


Figure 3. Hot Swap Control for I/O & Core Supplies

allowing a higher circuit breaker threshold at startup and a lower threshold after the supply current has settled. The circuit breaker also provides dual level and dual response time functions for overcurrent protection by integrating a slow and a fast comparator. This further enhances the circuit breaker performance by differentiating between slight overcurrent faults or catastrophic short circuit conditions.

The precise performance of the LTC4213 makes it ideal for systems requiring continual protection of low voltage supplies. Offered in the tiny 3mm x 2mm 8-lead DFN and 8-lead SOT-23 packages, it offers an extremely small overall solution size for mezzanine cards and small form factor cards.

Ultralow Voltage Dual Hot Swap Controller

Whereas the LTC4213 and LTC4216 support one switched supply voltage, the LTC4221 applies to systems with two switched supplies. This dual Hot Swap controller features a dual-level circuit breaker and the ability to control a core supply voltage as low as 1V (see Figure 3). The dual-level circuit breaker offers an adjustable filter for moderate overcurrent faults, yet responds immediately to catastrophic faults such as a short-circuit. The circuit breaker threshold of only 25mV minimizes the potential voltage drop for the core supply of the latest generation of dual-voltage FPGAs, ASICs and processors. In addition to active inrush current limiting for live insertion, the LTC4221 protects the processor from latch-up due to supply sequencing problems. With separate ON inputs, separate high side gate drivers for N-channel MOSFETs and separate power good outputs, the LTC4221 allows the user to configure the system for either simultaneous or sequenced I/O and core voltage ramping.

The output voltages are monitored through multifunction feedback pins. During ramp-up, the inrush current limit folds back as a function of the output voltage to protect the MOSFET. Once fully ramped up, the outputs are monitored for overvoltage and undervoltage faults as signaled by the FAULT and PWRGD pins. In the event of an overcurrent fault on either the I/O or core supply, both supplies respond and optionally retry or remain latched off to further protect the system.

Hot Swap Control with Digital Monitoring

In complex high availability applications, it is increasingly important to monitor system power for two reasons. First, you can watch for anomalous trends over time that indicate abnormal operation and anticipate impending failures. Second, systems commonly allocate power between different card types to economize on total power supply capacity. Power monitoring ensures that the cards stay within their allotment. Residing at the power connector, the Hot Swap circuit is a natural place to monitor the power entering a card.

The latest generation of Hot Swap controllers, such as the LTC4215 in Figure 4, make power

Low Voltage Hot Swap Control

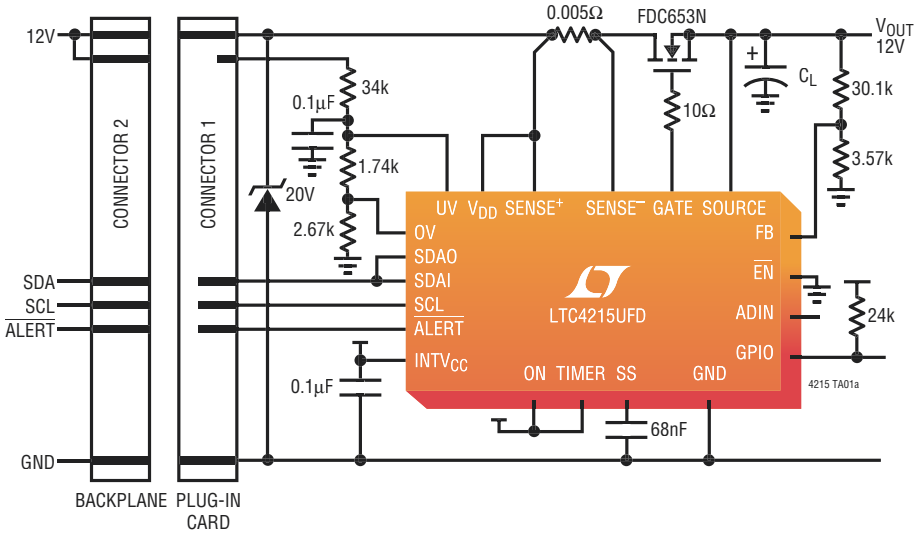


Figure 4. Hot Swap Control with Integrated Digital Power Monitoring

monitoring easy. In addition to the core Hot Swap functions of inrush current control and electronic circuit breaker, it incorporates an 8-bit analog to digital converter, multiplexer, preamplifier circuitry, and digital interface that enable an unprecedented level of monitoring and control. Knowing voltage and current lets you determine power in the card and observe trends.

In high-availability systems, careful monitoring of the health and integrity of the power distribution network is crucial. Information in the ADC registers can be queried via the I²C™ bus and then used to determine if a card is actually using its allocated power, or operating abnormally. An irregular card can be flagged for service even before it fails.

The LTC4215 turns the board supply voltage on and off in a controlled manner. It offers adjustable dI/dt softstart and provides active current limiting that results in a controlled supply ramp. The inrush current and circuit breaker limits, as well as the undervoltage/overvoltage thresholds, are independently adjustable, ensuring maximum flexibility and accuracy. The controller disconnects the load if it remains in current limit beyond the time-out delay and can be configured to latch off or auto-retry following the event.

The LTC4215 has additional features to interrupt the host when a fault has occurred, notify when output power is good, detect insertion of a board and turn off the pass transistor if an external supply monitor fails to indicate powergood within a timeout period.

Conclusion

Safely managing power during live insertion of cards is a critical feature of high availability systems. Reducing the electronic circuit breaker threshold to 25mV across the sense resistor or using V_{DS} sensing across the MOSFET dramatically improves the efficiency of using a Hot Swap controller for high current, ultralow voltage supplies in a mezzanine or backplane environment. Hot Swap controllers from Linear Technology support these applications with optimized features, from basic electronic circuit breaker functions to digital power monitoring.

BY REZA MOGHIMI • ANALOG DEVICES

Effective use of IC-amplifier macromodels requires understanding their limitations

SOMEDAY, IC MANUFACTURERS MAY PROVIDE USERS WITH AMPLIFIER MACROMODELS THAT ARE AS DETAILED AS THOSE THAT DEVICE DESIGNERS USE. UNTIL THEN, YOU MUST MAKE DO WITH LESS DETAILED MODELS, WHOSE EFFECTIVENESS DEPENDS ON YOUR UNDERSTANDING OF THEIR LIMITATIONS.

What should you expect from an amplifier macromodel? Almost every semiconductor manufacturer provides Spice models for its amplifiers, but no standards exist for these models. So, which specs do these devices model, and how accurate are those models? All designers have run circuit simulations. Some run simulations to verify that their design idea works correctly or whether they are overlooking some fundamental aspect of the circuit, such as exceeding the amplifier's maximum input or output range. Some run simulations to better understand how a circuit works. In all cases, the answers they get from the simulations are only as accurate as the circuit's least-accurate device model.

Amplifier-IC designers use detailed models to design their circuits. Transistor models can contain more than 50 parameters, reflecting the level of performance that is available from a given process. These detailed models give more accurate results than does fabricated silicon. So, why don't manufacturers give these same models and circuits to customers? Computing power and storage space are exponentially higher today than in the early days of macromodeling. The PCs on most designers' desks can handle the computational complexity for such dense models—designs that once could practically run only on workstations. The details of the circuit design and the process technology are proprietary, however, so manufacturers are usually unwilling to provide transistor-level models.

The future of amplifier and analog-component macromodeling may well lie in manufacturers providing customers with black-box equivalents. Such macromodels would use the same detailed transistor models that IC designers use, except that the models would use encryption to avoid reverse-engineering of the exact design (**Figure 1**). This scheme is interesting because it eliminates almost all of the uncertainty in customer simulations; the macromodels would be as accurate as the IC vendor's internal models. The challenge in developing such macromodels would lie not in encrypting their insides, but in providing the necessary software hooks to integrate them as subcircuits into the Spice simulator. Until such encrypted models exist, designers must continue to work with available simplified macromodels, keeping in mind what they should expect from them.

WHAT TO EXPECT FROM AN OP-AMP MODEL

A professor once advised his students never to run a simulation without having an idea of the expected results. That advice is good. The simulation may not turn out the way you expected, at which point you can question either your understanding or the result. However, with no expectation, you won't know whether the result makes sense. Almost all amplifier macromodels accurately simulate open-loop gain versus frequency and phase margin. Phase margin is important to modeling stability, step-response overshoot, and settling time. Most macromodels correctly reflect phase margin, which improves as the amplifier's closed-loop gain increases. However, some macromodels paint an inaccurate picture of how phase margin decreases with capacitive load. The macromodel shows phase margin decreasing as capacitive load increases but probably not at the same rate as in the real amplifier. The difference is understandable, because accurately determining phase margin requires good modeling of output impedance versus frequency and the exact locations of the amplifier's secondary

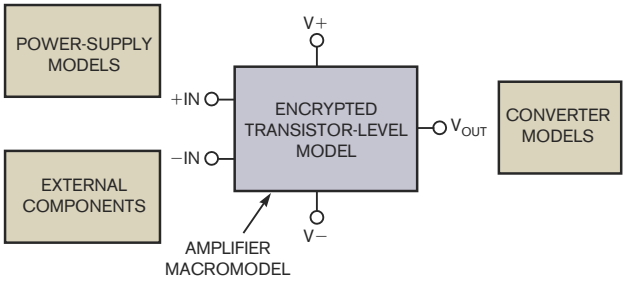


Figure 1 In the future, macromodels for customer use may contain the same detailed device models as those that IC designers use, except that the customer versions will use encryption to prevent reverse-engineering of the devices.

poles and zeros. Such accuracy is too much to expect from a simple macromodel.

Macromodels generally provide accurate models of CMRR (common-mode rejection ratio) and supply current versus supply voltage. One downside to today's simplified macromodels is that they don't always model breakdown voltages. You can apply supply voltages to the model higher than those you can safely apply to the real device and not observe the problems the real device would exhibit. One thing to question is the validity of supply-current simulations at supply voltages below the amplifier's specified supply range. Most macromodels use independent voltage and current sources to bias internal nodes in the subcircuit. This approach causes simulated current flow through the model even with a 0V supply. The basic rule is that you can expect reasonable accuracy if you simulate within the device's normal operating conditions.

RAIL-TO-RAIL AMPLIFIER MODELS

The last 10 years have brought an increase in the number of rail-to-rail amplifiers. Rail-to-rail inputs allow the input-common-mode-voltage range to extend to—and, in many cases, reach at least 200 mV beyond—the supply voltages. Unfortunately, many macromodels do not accurately simulate this behavior. You achieve rail-to-rail input by placing an NMOS or NPN differential pair in parallel with a PMOS or PNP differential pair. Although most macromodels use a similar parallel structure in their subcircuits, they do not deactivate the input stages once they exceed the critical common-mode voltage. The resulting macromodel allows high or low input and still provides valid outputs. This error presents no problem in simulations of normal input conditions. However, the simulation doesn't show what could be a potential real-life problem: the amplifier's true behavior when you apply a non-nominal input.

Output saturation voltage is the difference between the maximum or minimum output voltage and the supply rail. As output source current increases, so does output saturation voltage. For CMOS amplifiers, this relationship is linear. Another real-life aspect of rail-to-rail-output amplifiers is that their dc open-loop gain is proportional to the load resistance. Conversely, the dominant-pole frequency is inversely proportional to load resistance; hence, the gain-bandwidth product remains constant as the load resistance changes. Most rail-to-rail-output macromodels don't show this effect.

The fundamental reason for the inaccuracy is that most macromodels base their output stages on the Boyle model architecture (**Figure 2** and **Reference 1**). Although the architecture is effective for non-rail-to-rail-output stages, it does not account for the change in maximum output or maximum input voltage as the output current changes. It also doesn't account for the change in dc open-loop gain or a dominant-pole frequency that depends on load resistance.

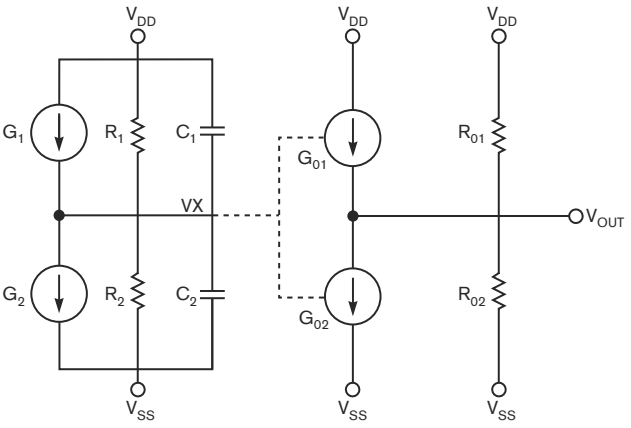


Figure 2 This simplified Analog Devices PSpice-model output stage is effective for non-rail-to-rail outputs, but it accounts for changes in neither the maximum or minimum output voltage as the output current changes nor the load resistance's effect on dc open-loop gain or dominant-pole frequency.

One architecture, however, accounts for all of these properties (**Figure 3**). This Analog Devices PSpice model uses an active output stage and is similar to the one that real rail-to-rail-output amplifiers use. **Figure 4** shows the simulated output-saturation voltage using Analog Devices' AD8656 macromodel. **Figure 5** shows actual measurement data for the AD8656. The results compare nicely. The test circuit configures the amplifier macromodel for an inverting gain of 10 with a dc-input signal sufficient to push the output voltage to the supply rail. The output of the amplifier connects to an independent current source. The current source uses dc analysis for sweep. The output-saturation voltages are the voltage differentials between drain-to-drain voltage and output voltage with the output-sourcing current and between the output voltage and source-to-source voltage when the output is sinking current.

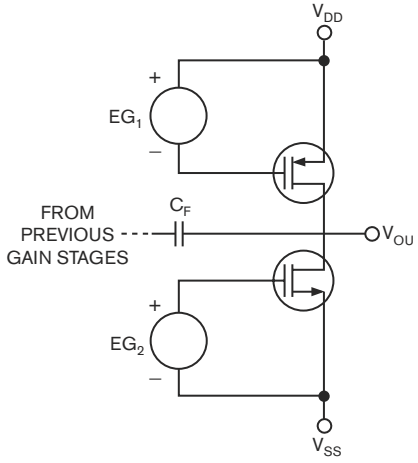


Figure 3 The Analog Devices PSpice model uses an active output stage similar to those that real rail-to-rail-output amplifiers use.

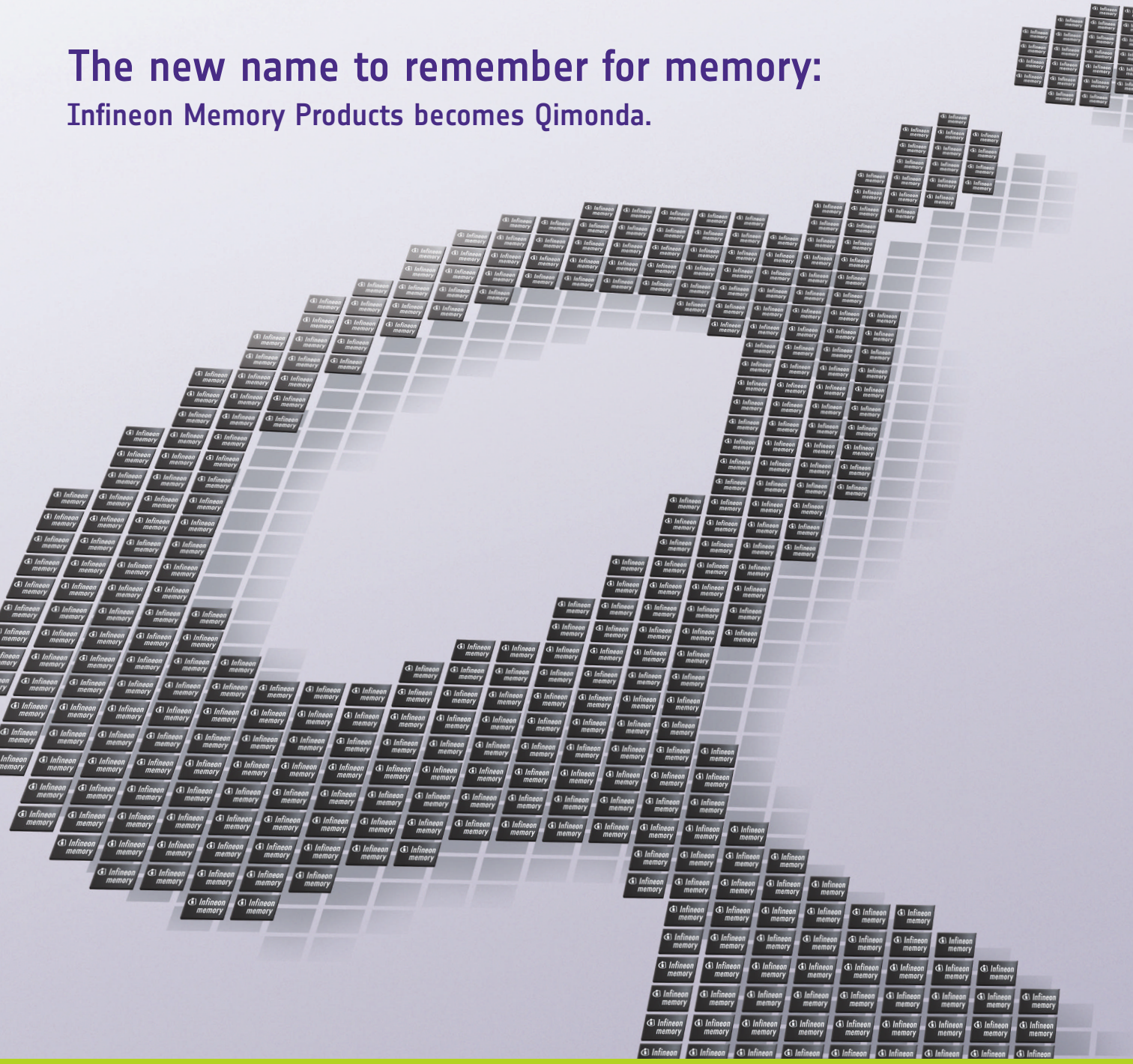
MODELING NOISE

Most models are reasonably accurate at modeling broadband-voltage noise. Some account for current noise, as well. In general, current noise is a concern only if you are using a bipolar-input amplifier and external resistances around the amplifier are 100 kΩ or greater. An amplifier macromodel may not do a good job of modeling flicker, or 1/f, noise, or it may not model it at all. This shortcoming is probably unimportant if the upper limit of the bandwidth of interest is higher than 5 kHz. CMOS and JFET amplifiers tend to have 1/f corners of hundreds of hertz compared with bipolar amplifiers' corners of several hertz, so having an inaccurate flicker-noise model may not be a problem.

Models never perform analyses of noise versus time. Spice performs noise simulations using ac analysis with the noise

The new name to remember for memory:

Infineon Memory Products becomes Qimonda.



We're concentrating on our core business – integrated memory solutions. With technological expertise, innovative design and more than 12,000 highly motivated staffers worldwide, we develop groundbreaking products for our customers.

Qimonda stands for creativity, passion, speed and our vision: We are the world's leading creative memory company.

www.qimonda.com

qimonda

option turned on. Transient analysis does not show the random-noise fluctuations visible on oscilloscopes. Spice provides no randomization function for independent sources, so no easy way exists to model noise versus time.

CREATING YOUR OWN MODEL

Spice treats every resistor as a noise generator. It models this thermal noise as an ideal noiseless resistor in series with a voltage source, E_N, of spectral density: $E_{NRMS}=\sqrt{kTR}$ in volts per the square root of hertz, where k is Boltzmann's constant, T is the absolute temperature in degrees Kelvin, and R is the resistance in ohms. You can create a noiseless resistor by modeling the resistor as a current-dependent voltage source. This approach is useful for evaluating noise contribution of sections or for isolating macromodel noise. Given a resistor with a value of res_value connected between nodes 1 and 2, substitute the following code: HN 1 3 VSN res_value, and VSN 3 2 DC 0, where HN is a current-controlled voltage source, and VSN is a 0V independent voltage source. The current through VSN is the dependent variable for the H-source. VSN is necessary only because Spice does not allow H-sources to be self-referencing. This characteristic is something of an oddity because G-sources can be self-referential.

You can easily create a broadband noise source that produces 1 nA/$\sqrt{Hz}$ of noise at 27°C. Connect this resistance across a 0V V-source and use an H-source whose output voltage depends on the current through the V-source. The gain of the H-source sets the desired voltage-noise level in nanovolts per the square root of hertz. This technique is common in amplifier macromodeling. The following example creates a 5.4-nV/$\sqrt{Hz}$ broadband noise source: Rnoise 1 0 16.45m, Vsense 1 0 DC 0, Hnoise 2 0 Vsense 5.4. Remember, the voltage-noise level increases with the square root of temperature.

You can create a flicker-noise source, as well. Some sample circuits in PSpice books incorrectly model 1/f noise. Flicker noise decreases with increasing frequency at a rate of −10 dB/decade. Therefore, you cannot model flicker noise with a simple RC filter; one-pole filters attenuate at a rate of −20 dB/decade. To model flicker noise, create a circuit similar to that for broadband noise, but use a diode instead of a resistor. The following **equation** yields the diode's flicker-noise current: $I_N=\sqrt{KF\times I_D^{AF}}$ in amps per the square root of hertz, where I_D is the dc current through the diode, and KF and AF are set in the diode's "model" statement. The default value of AF is 1; adjust KF to set the desired flicker-noise level.

You set the V_{SENSE} source and I_S in the diode-model statement to produce a 1-mA current through the diode. Because the diode model also generates shot noise—broadband noise that increases with the square root of I_D—minimize the diode current. Diode current of 1 mA generates approximately 18 pV/$\sqrt{Hz}$ of shot noise, which should be sufficiently low. Dflick 1 0 DNOISE, Vsense 1 0 DC 0.6551, Hnoise 2 0 POLY(1) Vsense 1m 1, and .MODEL DNOISE(IS=1E−14,KF=7.23E−10).

The constant term of the H-source, POLY(1), removes the 1-mA dc-current dependence, whereas the second term reflects the current through V_{SENSE} as an output voltage. This example provides enough flicker noise to create a 1/f corner frequency of 100 Hz, given a separately established broadband noise of 85 nV/$\sqrt{Hz}$. Adjust KF to change the 1/f corner; the corner is directly proportional to KF.

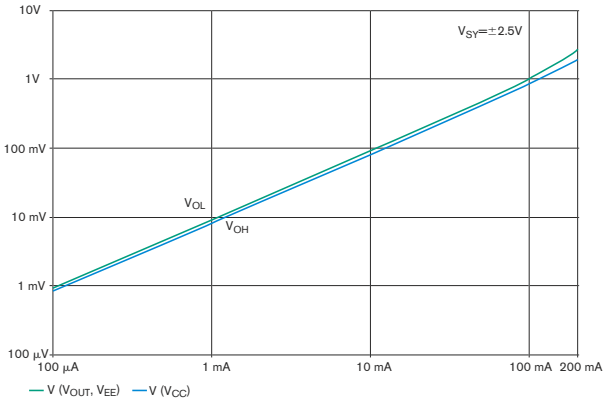


Figure 4 The curve of simulated output-saturation voltage versus output current from the AD8656 macromodel is highly linear.

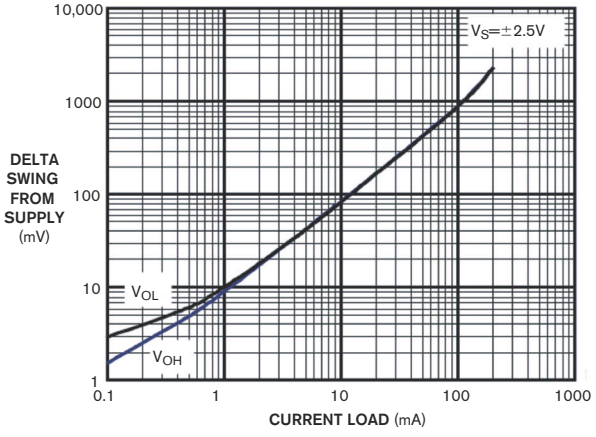


Figure 5 As the data sheet shows, the real AD8656's output-saturation voltage versus output current is similar to the figure that the macromodel predicts (see Figure 4).

Amplifier models for customers will continue to evolve and improve to provide the best accuracy. System designers should hold semiconductor vendors' amplifier models to higher standards. A future possibility is for semiconductor vendors to provide black-box models that use the same detailed transistor circuits that IC designers use. These black-box models must use encryption to protect intellectual property yet still be able to easily connect to Spice simulators. Until such models become available, you need to understand the limits of existing amplifier models. EDN

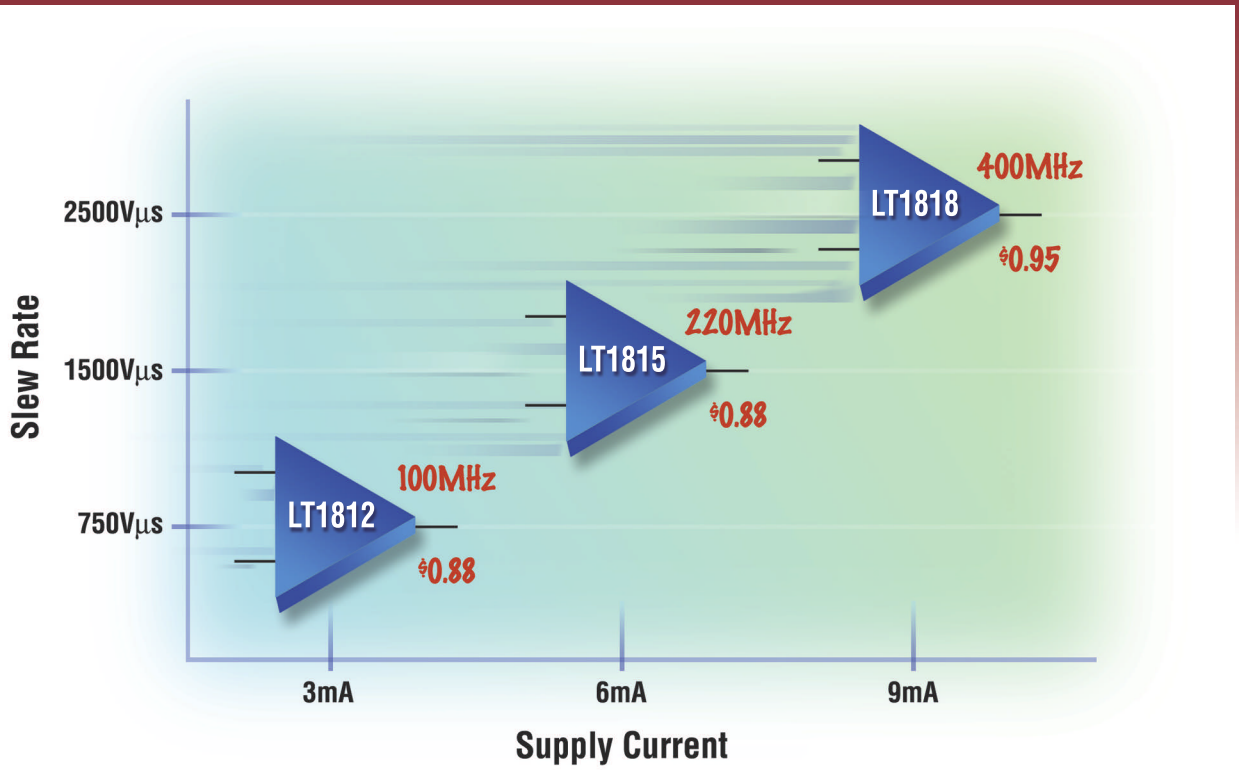
REFERENCE

1 Boyle, GR, DO Pederson, BM Cohn, and JE Solomon, "Macromodeling of integrated circuit operational amplifiers, *IEEE Journal of Solid-State Circuits*, Volume SC-9, No. 6, December 1974.

AUTHOR'S BIOGRAPHY

Reza Moghimi is senior applications engineer for Analog Devices' precision-analog-products group and audio group (San Jose, CA). He has a bachelor's degree in electical engineering from San Jose State University, as well as a master's degree in business administration. His hobbies include traveling, listening to music, and playing soccer.

Fast & Affordable



High Speed, Low Noise & Excellent AC/DC Performance for Less than $1.00

Unprecedented performance at an unbeatable price! The LT®181X family of high speed amplifiers offers bandwidth up to 400MHz, slew rates as high as 2500V/µs, noise less than 6nV/√Hz and distortion as low as –92dBc. Operating on either single 5V or ±5V supplies, the LT181X family is ideal for video and RF amplification, communication receivers, cable drivers, and data acquisition systems. Space-saving SOT-23, DFN, MSOP and SSOP packaging is available.

High Speed Voltage Feedback Op Amps

Part Number	Channel	SR	GBW	e_n	HD@1MHz	I_{OUT}	I_S	1k Price
LT1818/9	S/D	2500V/µs	400MHz	6nV/√Hz	-92dBc	200mA	9mA	$0.95/$1.60
LT1815/6/7	S/D/Q	1500V/µs	220MHz	6nV/√Hz	-80dBc	200mA	6.5mA	$0.88/$1.50/$2.05
LT1812/3/4	S/D/Q	750V/µs	100MHz	8nV/√Hz	-80dBc	100mA	3mA	$0.88/$0.99/$1.95
LT6205/6/7	S/D/Q	450V/µs	100MHz	9nV/√Hz	-80dBc	60mA	3.75mA	$0.88/$1.05/$1.50
LT1722/3/4	S/D/Q	70V/µs	200MHz	3.8nV/√Hz	-90dBc	90mA	3.7mA	$0.88/$1.15/$2.19

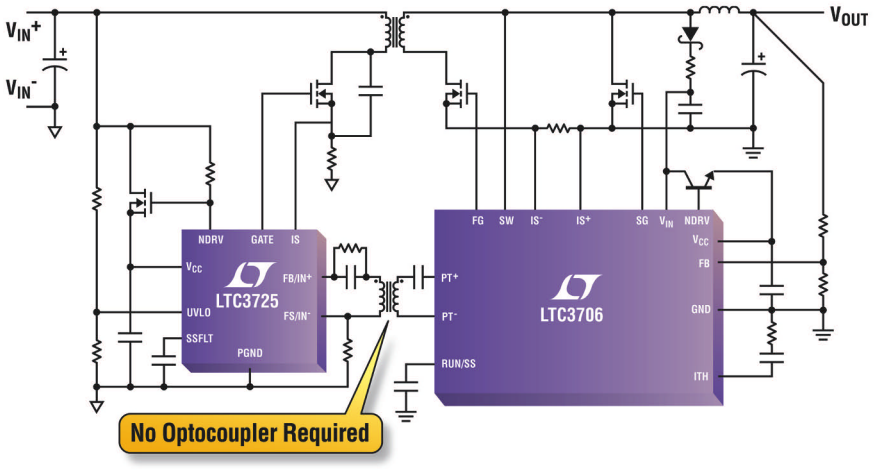
Info & Free Samples

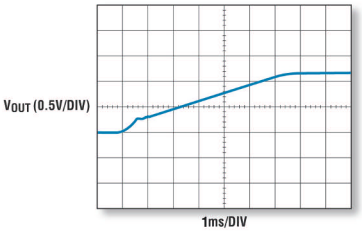
www.linear.com/181X
Literature: 1-800-4-LINEAR
Support: 408-432-1900

LEAD-FREE RoHS COMPLIANT

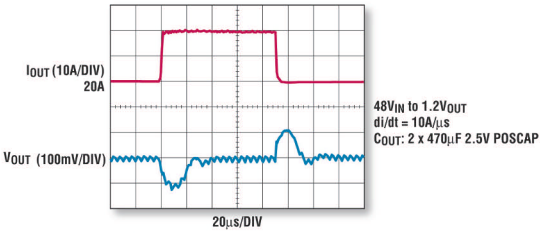
LINEAR TECHNOLOGY

Think Outside the Brick





Smooth, Well Controlled Start-Up



Fast "Buck" Transient Response with Secondary-Side Control

Simple, Fast, Flexible 48V Isolated Conversion

Designing an isolated DC/DC supply is now as straight forward as designing a buck converter. Linear's new smart primary-side drivers and secondary-side controllers simplify design of isolated supplies for single-step conversion from $48V_{IN}$ to a wide output voltage range and scalable load current: 0.6V to 52V at 10A to 200A.

Features

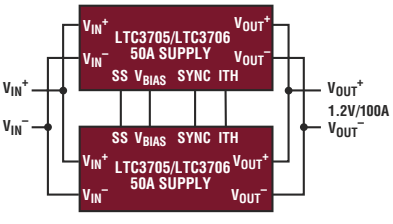
- Secondary-Side Control– Simplifies Feedback Loop
- Self-Starting Architecture– Eliminates Primary Bias Supply
- Output Voltages from 0.6V to 52V
- Current Sharing for Easy Upgrade to Higher Output Power
- Available Pb-free and RoHS Compliant or in Standard SnPb Finish

Primary Side:

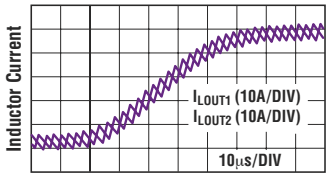
LTC®3705: Two-Transistor Gate Driver
or
LTC3725: One-Transistor Gate Driver

Secondary Side:

LTC3726: Single and PolyPhase® Synchronous Forward Controller
or
LTC3706: Full-Featured LTC3726



Scalable Design with PolyPhase Operation for Higher Power



Exceptional Current Sharing During 1.2V, 100A Load Current Step

Info & Free Samples

www.linear.com/isopower
Literature: 1-800-4-LINEAR
Support: 408-432-1900

LINEAR TECHNOLOGY

EDITED BY BRAD THOMPSON
AND FRAN GRANVILLE

designideas

READERS SOLVE DESIGN PROBLEMS

JFET cascode boosts current-source performance

Clayton B Grantham, Tucson, AZ

Many process-control sensors, such as thermistors and strain-gauge bridges, require accurate bias currents. By adding a single current-setting resistor, R_1, you can configure voltage-reference circuit IC_1 to produce a constant and accurate current source (**Figure 1**). However, the source's errors depend on the accuracy of both R_1 and IC_1 and affect measurement accuracy and resolution. Although you can specify high-precision resistors whose accuracy exceeds that of most commonly available voltage-reference ICs, the voltage reference's error dominates this current source's accuracy. Although the manufacturer minimizes the voltage reference's temperature sensitivity and output-voltage error, sensitivity to power-supply variations can affect its accuracy, especially in process-control applications that must operate over a wide range of supply voltages.

A cascode-connected pair of JFETs, Q_1 and Q_2, form a constant-current source that minimizes the reference circuit's sensitivity to supply-voltage fluctuations and extends IC_1's operating voltage beyond its 5.5V maximum rating. In addition, Q_1 and Q_2 effectively increase the current source's equivalent resistance from a few megohms almost into the gigohm range. In the circuit's Norton model, equivalent resistance represents the parallel resistance across an ideal current source.

An N-channel JFET operates as a depletion-mode device at its maximum saturated drain current when its gate-to-source bias voltage is 0V. In contrast to a depletion-mode MOSFET that requires a gate-bias voltage to conduct, the JFET operates in a default on-state and requires gate-bias voltage to cut off conduction. As its gate-to-source voltage becomes more negative with respect to the source, a JFET's drain current goes to zero at the pinch-off voltage. The JFET's drain current varies approximately with its gate bias: $I_D \approx I_{DSS} \times (1+V_{GS}/V_P)^2$, where I_D is drain current, I_{DSS} is the sat-

DIs Inside

▶ What are your design problems and solutions? Publish them here and receive $150! Send your Design Ideas to edndesignideas@reedbusiness.com.

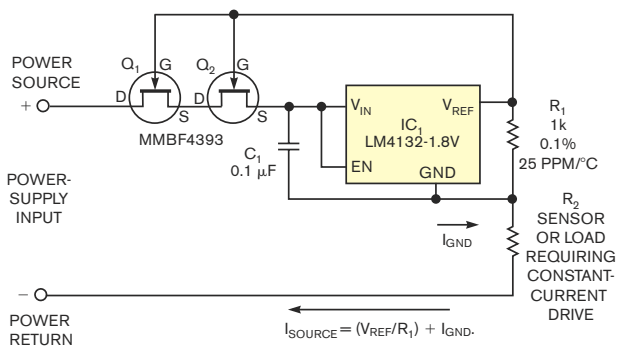


Figure 1 A pair of cascode-connected JFETs reduces the effects of power-supply-voltage fluctuations on a current source's accuracy.

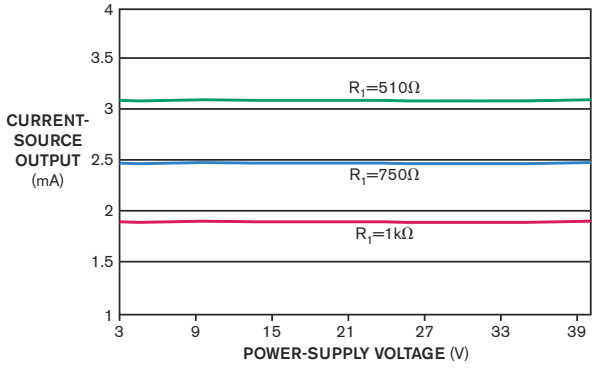


Figure 2 Setting R_1 to values of 1 kΩ, 750Ω, and 510Ω delivers output currents of approximately 1.8, 2.5, and 3.6 mA that are insensitive to a wide range of power-supply voltages.

urated drain current, V_{GS} is the gate-to-source voltage, and V_P is the pinch-off voltage.

Assume that IC_1's output voltage, V_{REF}, remains constant at 1.8V. Because the output voltage drives Q_2's gate, IC_1's input voltage, V_{IN}, equals $V_{REF}-V_{GS(Q2)}$, or $1.8V-(-1.2V)=3V$. Thus, Q_2's gate-to-source voltage rests at its nominal pinch-off voltage of 1.2V and varies in step with small changes in current source. As the power-supply voltage varies from 3V to more than 30V, then the input voltage remains almost constant, as you would expect, because V_{REF} also remains constant. The cascoded-FET configuration increases the current source's Norton equivalent resistance beyond that of the voltage reference and R_1 alone. You can use a single JFET, but stacking two JFETs further enhances the circuit's effective impedance. Note that IC_1 doesn't degrade accuracy because the JFETs hold IC_1's input voltage virtually constant, and IC_1 effectively cancels initial gate-to-source-voltage variations and temperature effects that Q_1 and Q_2 introduce.

Negative feedback in the Kirchhoff-voltage loop that comprises V_{IN}, V_{REF}, and $V_{GS(Q2)}$ allows the drain current to reach an equilibrium bias point that satisfies Q_2's transfer equation. Comprising the sum of (V_{REF}/R_1) plus IC_1's internal "housekeeping" current, I_{GND}, Q_2's drain current remains constant. Adding Q_1 reduces the effects of Q_2's output impedance to insignificance. Adjusting the value of R_1 varies the circuit's output current over a useful range of 200 µA to 5 mA, with Q_2's saturated-drain-current specification imposing an upper limit. If you select a JFET with higher saturated drain current, make sure not to exceed Q_1's maximum power dissipation.

Note that the circuit's lower power-supply-voltage limit must exceed the circuit's compliance voltage, 3V, plus the voltage drop that the sensor introduces: $I_{SOURCE}\times R_2$. The circuit's upper power-supply voltage must not exceed $I_{SOURCE}\times R_2+30V$. For example, supplying a current of 2.5 mA to a 1-kΩ pressure-sensor bridge, R_2, limits the power-supply-voltage range to 5.5 to 32.5V. The circuit's output current varies less than 1 µA over a wide range of power-supply voltages (**Figure 2**). EDN

Microcontroller delivers voltage-multiplied dc power

Aaron Lager, Masterwork Electronics, Santa Rosa, CA

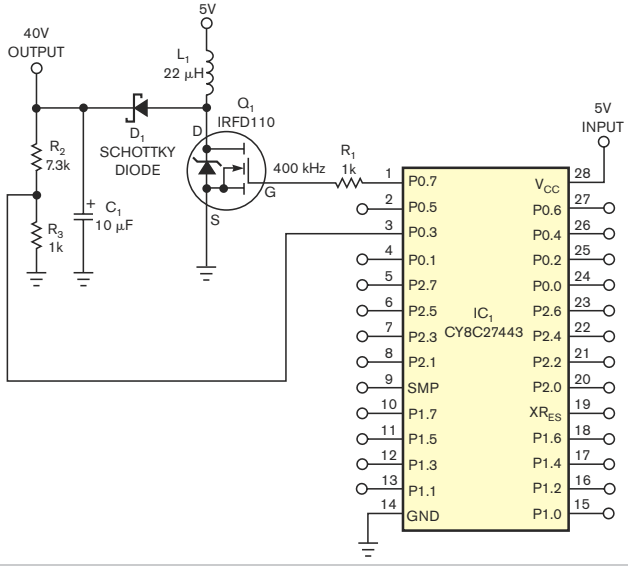
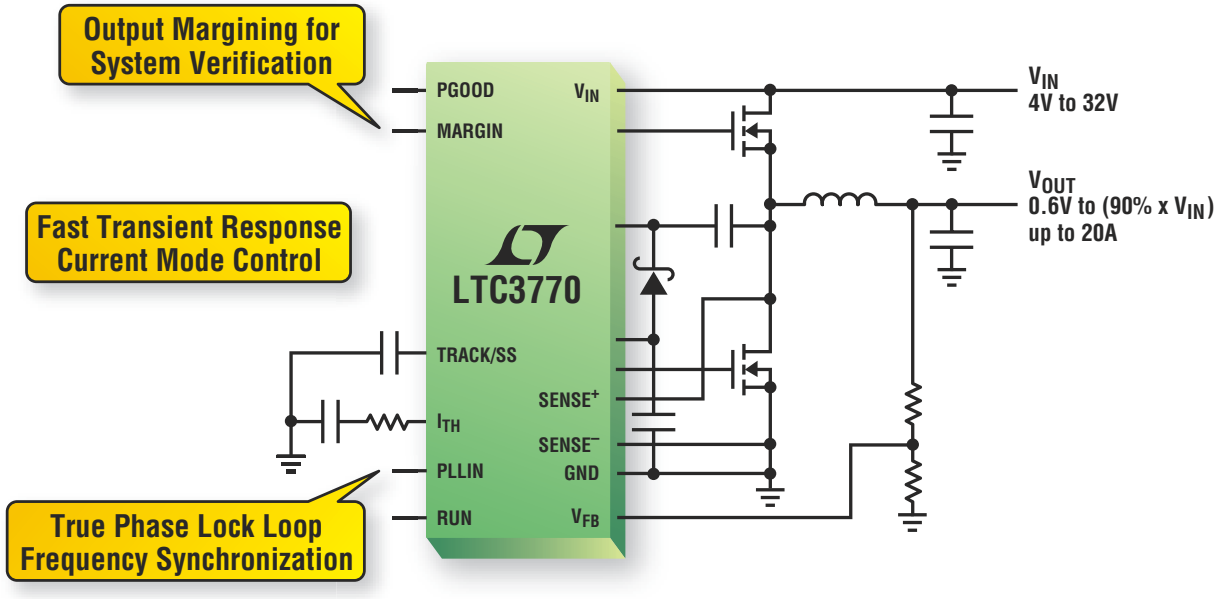


Figure 1 Use a pair of a PSOC microprocessor's internal blocks and a few external components to build a voltage-boost converter. Use a Schottky diode rated for a peak-inverse voltage of 100V for D_1. The PSOC's remaining pins are available for application support.

The combination of an external circuit and a low-voltage microcontroller occasionally requires a significantly higher power-supply voltage. You can use either an external boost converter to increase the logic supply or a buck converter to decrease an even higher voltage. However, you can alternatively use the microcontroller to create a higher voltage. For example, some of Cypress Semiconductor's (www.cypress.com) PSOC (programmable-system-on-chip) microcontrollers include a configurable comparator block that, with a PWM block, can form the heart of a simple inductor-based boost converter (**Figure 1**). A few external components implement a 40V power supply (**Figure 2**). When the feedback voltage you apply to Pin 3 (P0.3) exceeds the comparator's software-defined threshold voltage, the comparator shuts off the PWM stage. When the voltage drops below the threshold, the comparator re-enables the PWM block and thus regulates the output voltage. The voltage regulator uses only hardware blocks and

Accurate and Fast



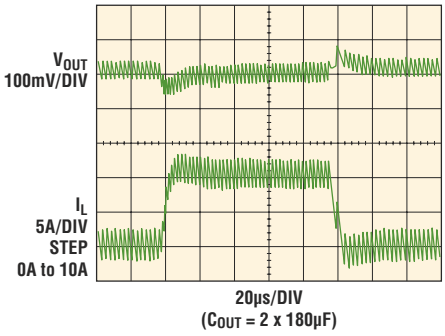
±0.67% Accurate at 0.6V_{OUT} Over Temperature

High performance servers, ASICs and computer memory systems demand very accurate, low voltage outputs. Fast transient response, up & down tracking and high efficiency operation are also necessary in these applications. Until recently, the only available solution required multiple ICs. Now there is the LTC®3770 - the newest member of our multifunction controller family. It's a synchronous step-down switching regulator controller with output voltage up/down tracking capability, voltage margining, high accuracy reference and fast transient response. The LTC3770 delivers all the performance these demanding applications require.

Features

- Wide V_{IN} Range from 4V to 32V
- Output Voltage Tracking Capability
- True Current Mode Control
- Sense Resistor Optional
- 2% to 90% Duty Cycle
- $T_{ON(MIN)} \leq 100ns$
- Adjustable Switching Frequency
- Adjustable Cycle-by-Cycle Current Limit
- 5mm x 5mm QFN and 28-lead SSOP Packages

Fast Transient Response



Info & Free Samples

www.linear.com/3770
Literature: 1-800-4-LINEAR
Support: 408-432-1900

LEAD-FREE RoHS COMPLIANT

LINEAR TECHNOLOGY

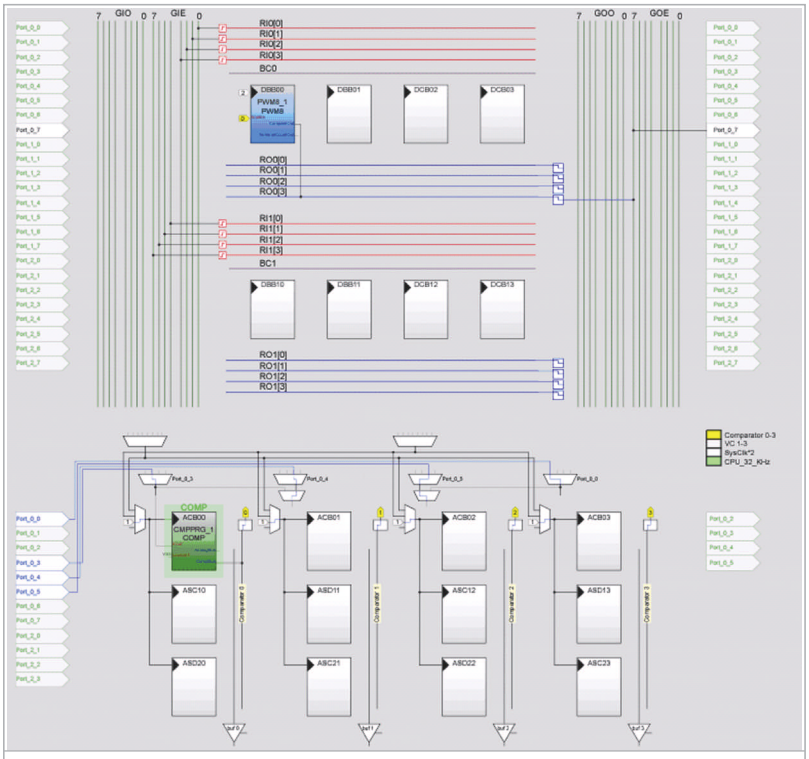


Figure 2 A pulse-width modulator (top) and a comparator (bottom) can operate independently of other PSOC functions. Unconnected pins are available for additional functions.

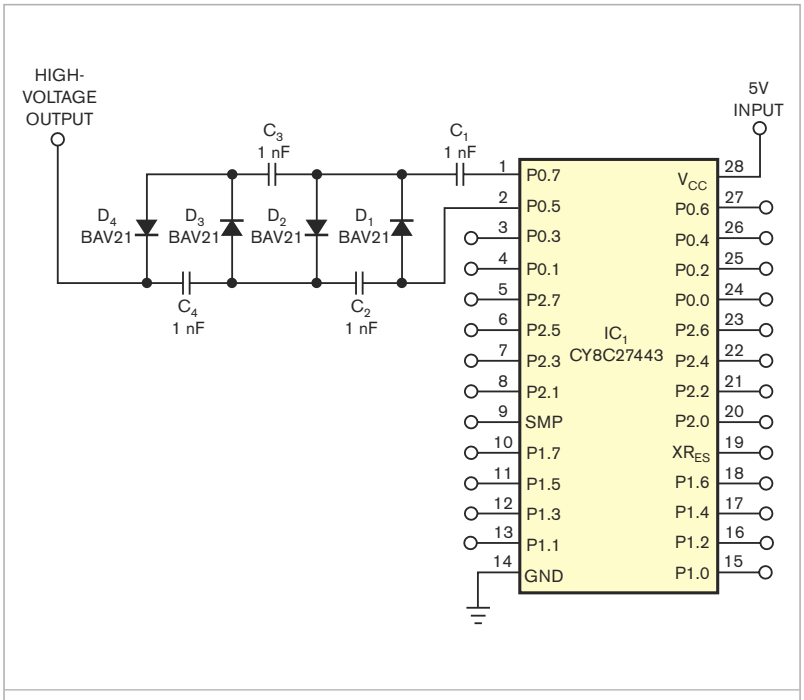


Figure 3 A few diodes and capacitors form a Villard Cascade voltage multiplier.

thus is immune to the effects of other activities taking place in the PSOC's CPU.

However, some microcontrollers lack a built-in comparator. For these devices, the Villard Cascade circuit offers a less expensive alternative to an external boost-voltage converter (**Reference 1**). Most engineers who are familiar with the Villard Cascade associate it with high-voltage applications and do not envision it as a low-voltage dc-supply technique. The circuit in **Figure 3** requires an ac input source that you can easily simulate using a PSOC's internal PWM and inverter blocks. A square-wave output voltage appears on Pin 1, and an inverted version of the same square wave appears on Pin 2. The voltage difference between the two pins applies an ac square-wave voltage to the cascade.

Figure 4 shows how to configure a PSOC's internal blocks to drive the circuit in **Figure 3**. The PSOC's output multiplexer inverts the PWM's output and drives Port_0_5, and Port_0_6 receives the PWM's noninverted output signal. Again, the PSOC uses hardware blocks to drive a Villard Cascade voltage multiplier, and the circuit produces an output voltage without regard to CPU activity. For an input voltage, V_{IN}, a Villard Cascade of N stages delivers an output voltage of $V_{IN} \times 2N$. One stage comprises two diodes and two capacitors (**Figure 5**). However, the series-connected capacitors and diodes introduce voltage drops that limit the output current available from a Villard Cascade. In addition, the following **equation** imposes a practical limit that governs the cascade's output voltage:

$$\Delta V = \frac{1}{fC}\left(\frac{2}{3}N^3 + \frac{1}{2}N^2 - \frac{1}{6}N\right),$$

where ΔV is the output-voltage drop, f is the input frequency, C is the capacitance, I is the output current, and N is the number of stages.

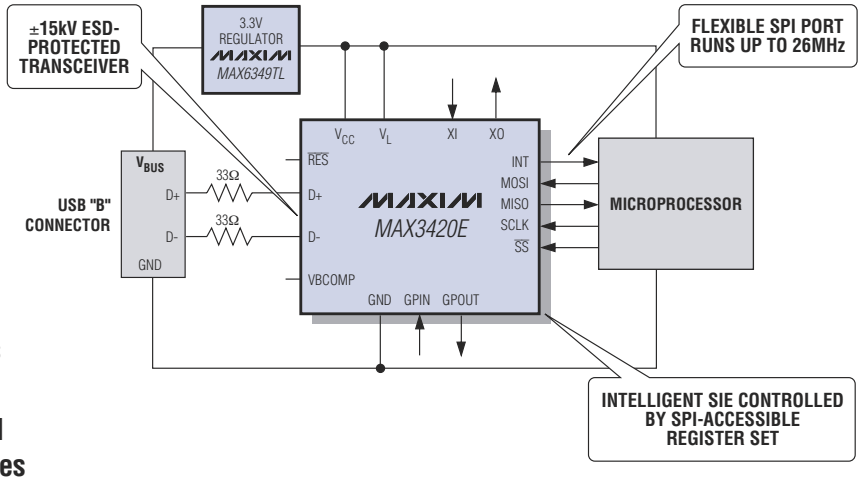
Both boost circuits can supply only modest amounts of current, especial-

ADD USB TO ANY SYSTEM

Make Your µP, DSP, or ASIC a Full-Speed USB Peripheral with the MAX3420E

Features

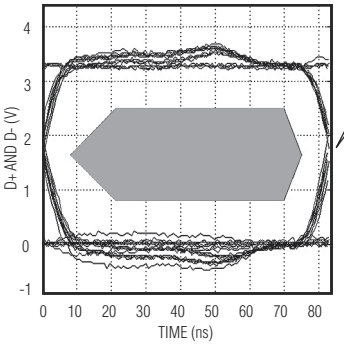
- ±15kV ESD-Protected, Integrated Full-Speed USB Transceiver (12Mbps)
- Programmable 3- or 4-Wire SPI™ Interface (Up to 26MHz)
- Easy to Program
- Integrated USB Serial Interface Engine (SIE)
- Extra I/Os: Four General-Purpose Inputs and Four General-Purpose Outputs
- Available in 24-Pin (4mm x 4mm) TQFN and 32-Pin (7mm x 7mm) TQFP Packages



Ideal for

- Industrial
- Meter Reading
- Automotive
- Medical

EYE DIAGRAM



CERTIFIED USB

FULL-SPEED (12Mbps) USB COMPLIANT

AVAILABLE IN SPACE-SAVING PACKAGES

24-TQFN

4mm x 4mm

SPI is a trademark of Motorola, Inc.

MAXIM

www.maxim-ic.com

FREE* Interface Design Guide—*Sent Within 24 Hours!

CALL TOLL FREE 1-800-998-8800 (7:00 a.m.–5:00 p.m. PT)
For a Design Guide or Free Sample

MAXIM/DALLAS DIRECT! DISTRIBUTION
1-888-MAXIM-IC

ARROW ELECTRONICS, INC.
1-800-777-2776

AVNET electronics marketing
1-800-332-8638

Distributed by Maxim/Dallas Direct!, Arrow, Avnet Electronics Marketing, Digi-Key, and Newark.

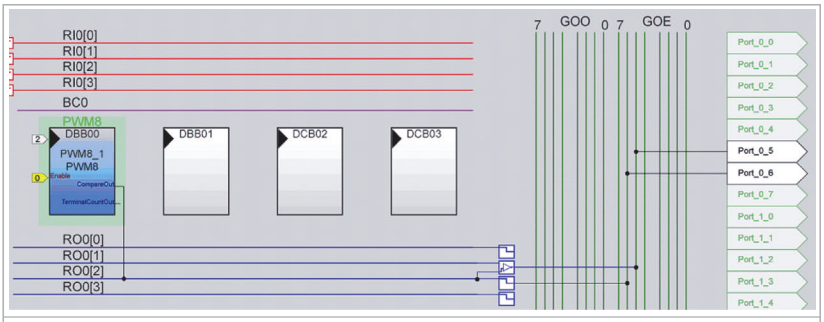


Figure 4 To drive a Villard Cascade multiplier, a PWM block and an inverter block deliver a balanced ac voltage with respect to ground.

ly when they receive power from a 5 or 3.3V source. However, you can charge a high-value storage capacitor from the boost circuit's output and drive a load that presents a low duty cycle (for example, solenoid actuation). EDN

REFERENCE

1 "Jochen's High Voltage Page," www.kronjaeger.com/hv/hv/src/mul/.

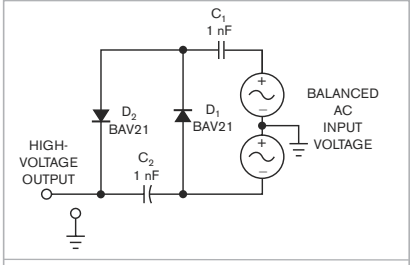


Figure 5 An isolated multiplier stage eases analysis.

Low-dropout linear regulators deliver constant currents

Budge Ing, Maxim Integrated Products Inc, Sunnyvale, CA

Linear voltage regulators offer a simple method of producing a constant current by connecting a fixed resistor between the regulator's output and ground nodes. The regulator's constant output voltage produces a constant current through the resistor. You can use the basic circuit as either a high-side or a low-side current source. The high-side current source uses a positive-output linear voltage regulator, IC_1, a Maxim MAX1818, to provide a constant current of 25 mA to the load resistance (**Figure 1**). The design imposes two conditions: First, the voltage between IC_1's V_{CC} and ground terminals must not exceed 5.5V. Second, the voltage between IC_1's input and ground terminals must meet or exceed 2.5V, the minimum voltage for proper operation. To satisfy these conditions, choose an output-resistance value that allows 2.5 to 5.5V between input and ground and provides a fixed output of 1.5V across the output resistance at the desired load current.

For example, if you use the circuit to drive a constant current through a 100Ω maximum load resistance while applying 5V V_{CC} between IC_1 and ground, the circuit functions properly when R_{OUT} equals or exceeds 60Ω. This value allows a maximum programmable current of 1.5V/60Ω, or 25 mA. The voltage across IC_1 then equals the allowed minimum: 5V−(25 mA×100Ω)=2.5V. Available in six-pin SOT-23 packages, the MAX1818 can source as much as 500 mA.

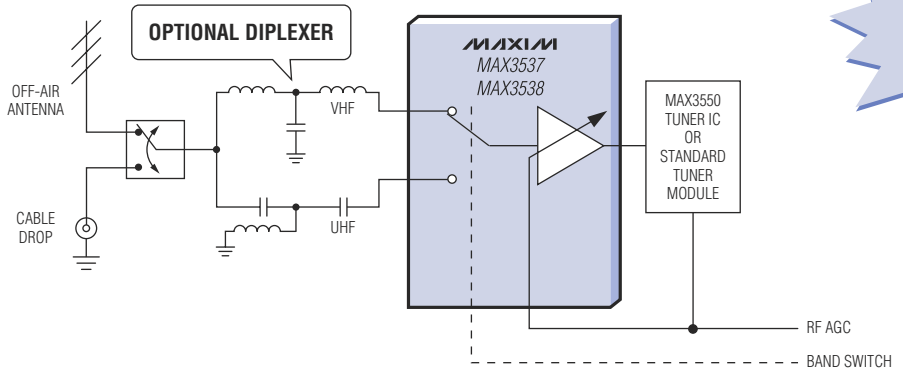
The low-side current-source circuit draws a constant current of 2.5V divided by the output resistance through the load resistance (**Figure 2**). In this example, IC_1, a MAX1735 linear negative-voltage regulator, provides a fixed output voltage of −2.5V. As in **Figure 1**, ensuring a voltage of 2.5 to 6.5V be-

VARIABLE-GAIN TV AMP DELIVERS WORLD-CLASS +18dBm IIP3 AT MAX GAIN

Innovative Switched-Diplex Filter Eliminates the Need for Expensive Baluns

MAX3537/MAX3538 are tailored for terrestrial TV set-top boxes and OpenCable™ TV front-ends where high linearity and low noise figure are important. Packaged in a 12-pin QFN and with 240mW power consumption, the MAX3538 outperforms the competition by providing unmatched linearity at less power consumption. The MAX3537 is targeted at lower performance, cost-sensitive applications, while the MAX3538 is designed for high-end applications.

12-QFN
4mm x 4mm x 0.8mm



NO BALUNS REQUIRED

MAX3538 Features

- ♦ Low Noise Figure—5.0dB at Max Gain
- ♦ High IIP3—+33dBm at 17dB Backoff
- ♦ High IIP2—+53dBm at 17dB Backoff

MAX3538/MAX3537 Benefits

- ♦ Single-Ended Inputs and Outputs—No Baluns
- ♦ Band Switch—Increases Effective IIP2

Part	Max Gain (dB)	AGC Range (dB)	Noise Figure (dB)	IIP3 at Max Gain (dBm)	Power Consumption (mW)
MAX3537	9.8	23.1	5.3	16.5	195
MAX3538	12.6	22.6	5.0	18.2	240

OpenCable is a trademark of Cable Television Laboratories, Inc.

MAXIM

www.maxim-ic.com/wireless

FREE* Wireless Design Guide—*Sent Within 24 Hours!

CALL TOLL FREE 1-800-998-8800 (7:00 a.m.–5:00 p.m. PT)
For a Design Guide or Free Sample

MAXIM DIRECT! DISTRIBUTION
1-888-MAXIM-IC

ARROW ELECTRONICS, INC.
1-800-777-2776

AVNET electronics marketing
1-800-332-8638

Distributed by Maxim/Dallas Direct!, Arrow, Avnet Electronics Marketing, Digi-Key, and Newark.

tween IC_1's ground and input terminals represents the only precaution for its proper operation. To satisfy that condition, choose an output-resistance value that allows 2.5 to 6.5V between ground and the input. When using the circuit to draw current through a maximum load of 100Ω with V_{CC} at 5V, the output resistance should exceed 100Ω, which provides a maximum programmable current of 2.5V/100Ω=25 mA, which in turn produces a minimum recommended voltage across the device of 5V−(25 mA×100Ω)=2.5V. The MAX1735 can source as much as 200 mA and occupies a five-pin SOT-23 package.

In addition to the programmed load current, both configurations allow the regulator's quiescent current to flow through the load and introduce a source of error that varies with the voltage you apply between the regulator's input and ground connections. You can minimize the error by choosing a voltage regulator that draws low quiescent current or whose quiescent current remains constant through the operating range and allows you to compensate the error by adjusting the value of the output resistance. Quiescent currents for the devices in **figures 1** and **2** typically average 130 µA and vary less than 40 µA for a regulator input-voltage range of 2.5 to 5V. EDN

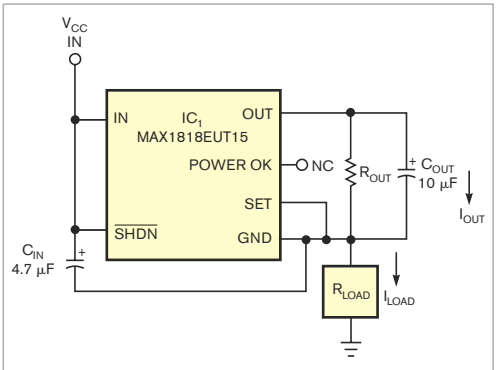


Figure 1 This high-side constant-current source delivers load current of 2.5V divided by the output resistance, provided that you choose the output resistance to ensure that the voltage between the regulator's input and ground terminals is at least 2.5V.

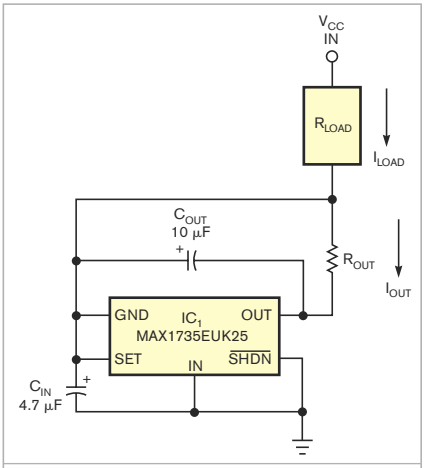
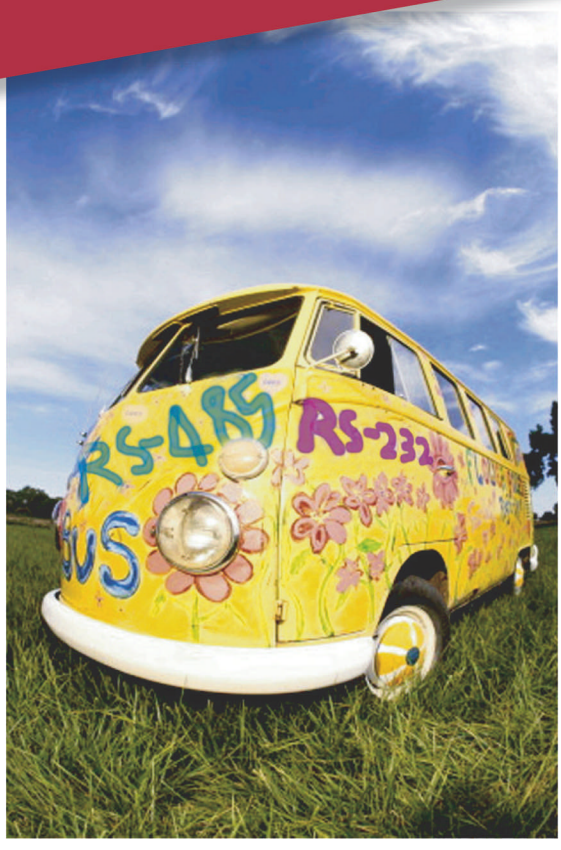


Figure 2 As in Figure 1, this low-side constant-current source draws a load current of 2.5V divided by the output resistance through the load resistance, provided that you select the output resistance to make the voltage difference between IC_1's input and ground terminals at least 2.5V.

Intersil Interface Products

High Performance Analog

Here Comes The Magic Bus!

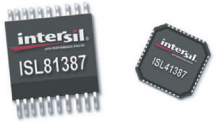


A single bus interface component that can operate on two different standards makes everything groovy. When that IC features on-chip 15kV ESD protection, it's magic. That was the thinking behind Intersil's new family of **±15kV ESD protected, Dual Protocol (RS-232/485) Interface Transceivers.**

Remember when your bus would have multiple features and functions - transportation, dining room, music studio, bedroom? Well, our new family of Dual Protocol Interface Transceivers, available in dual and single port, has everything you need in a transceiver.

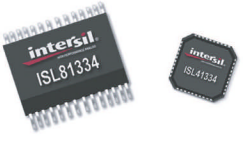
SINGLE PORT

2.2V min. Tx output voltage for exceptional noise immunity in RS-485/422 protocols and 1Mbps Rx data rate in RS-232 mode.



DUAL PORT

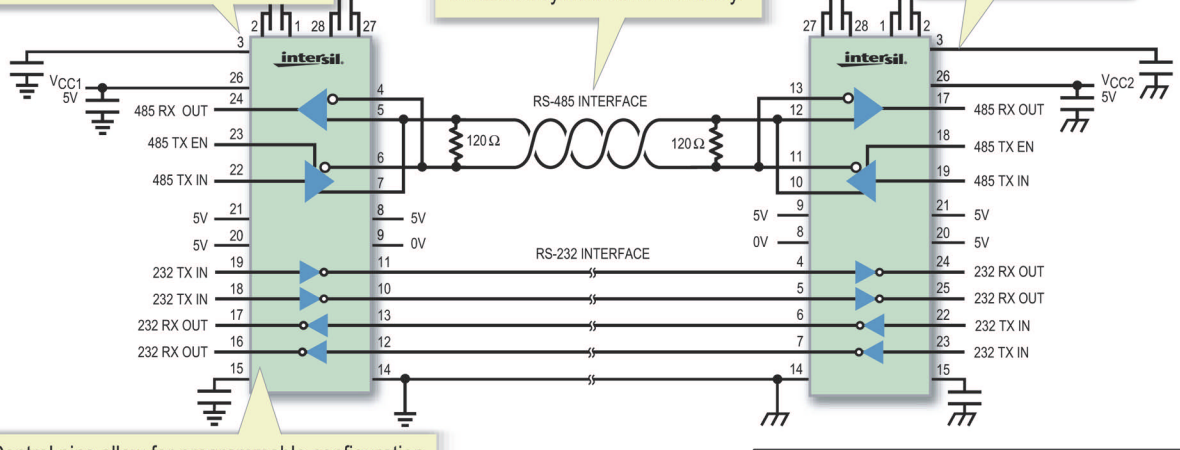
Additional ports on two-channel transceivers allow option for two RS-485/422 transceivers **or** four RS-232 transceivers.



Full fail-safe function guarantees a high level receiver output if the receiver inputs are floating or shorted.

Exceptional RS-485/RS-422 differential V_{OUT} (2.7V-3.1V) for increased system noise immunity.

Bus pins carry 15kV HBM protection.

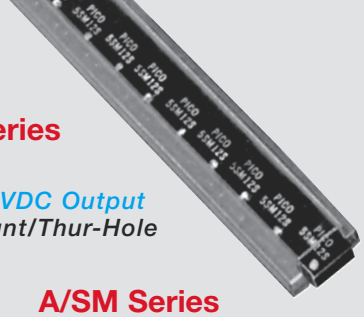


Control pins allow for programmable configuration to single RS-485/RS-422 or dual RS-232.

Datasheet, samples, evaluation boards and more information available at **www.intersil.com**

Intersil – Amplify your performance with advanced signal processing.

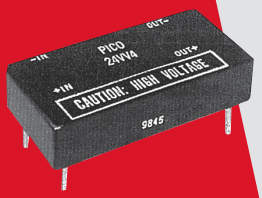
intersil®
HIGH PERFORMANCE ANALOG



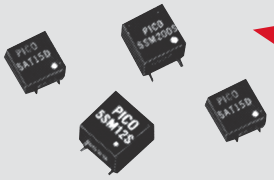
New AV Series
Isolated
100 to 5000 VDC Output
Surface Mount/Thur-Hole

New Dual Isolated Outputs
to 250 VDC Isolated Output
Thru-Hole and Surface Mount

VV Series
Up to 10,000 VDC Output
Up to 10 Watts



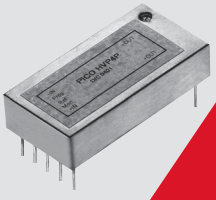
A/SM Series
Surface Mount/Thur-Hole
Isolated
3.3 to 1000 VDC Output



AVR Series
Regulated to IKV
Low Noise

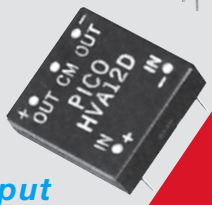
M/MV Series
Military Components
Military Environmental
Testing Available
3.3 to 500 VDC

HVP Series
Programmable to
6000 VDC Output

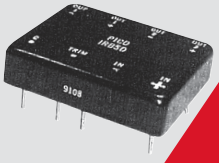


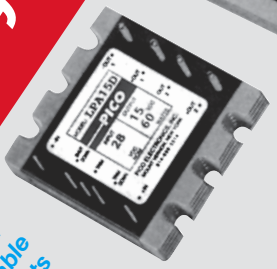
P/HP/XP Series
HIGH POWER
3.3 to 350 VDC
Output
Isolated to
300 Watts

LV/HV Series
36 to 170 Inputs
Terminal Strips
PC Board Mount
3.3 to 48 VDC Output



OR/IR/JR/KR Series
Wide Input Range
8 to 60 VDC
2 to 100 VDC Output
Regulated





LF/LM/FM Series
-40° and -55° to +85°C
Operating Temperature

3.3 to 350 VDC outputs
in 1/2 Brick and Full Brick

LP Series
Wide Input Range
Watts to 75 Watts
2 to 100 VDC Output Full Brick

DC-DC Converters
2V to 10,000 VDC Output

2500 Standard Models
Regulated/Isolated
Wide Input Available
1 Watt to 300 Watts

- **COTS**
- **MILITARY**
- **INDUSTRIAL**

Also AC-DC single and/or 3 Phase. Power Factor Corrected. 3 Watts to 2000 Watts Models.

PICO ***Electronics, Inc.*** 143 Sparks Ave. Pelham, NY 10803

• ***Call Toll Free*** 800-431-1064 • ***Fax:*** 914-738-8225

ISO CERTIFIED 9001:2000

SURFACE MOUNT • MILITARY UPGRADES • 2500 Standard Models • Custom Models

www.picoelectronics.com

E-mail: info@picoelectronics.com • ***Send for free 180 pg PICO Catalog***

LINEAR TECHNOLOGY

DESIGN NOTES

Wide Input Range 1A LED Driver Powers High Brightness LEDs with Automotive and 12V_{AC} Supplies – Design Note 388

John Tilly and Awo Ashiabor

Introduction

Today's ultrabright LEDs far exceed the performance of incandescent bulbs in both efficiency and lifetime. Taking full advantage of these features requires a correspondingly efficient and reliable LED driver, such as the LT®3474. The LT3474 is a step-down 1A LED driver that supports a variety of power sources, has a wide 4V to 36V input voltage range and is programmable to deliver LED current from 35mA to 1A at up to 88% efficiency. It requires minimal external circuitry and is available in a space saving 16-lead TSSOP package.

Automotive LED Driver

Figure 1 shows the configuration of the LT3474 operating from a 12V automotive battery input. As shown, the circuit can tolerate voltage swings from 4V to 36V, common in an automotive environment. With an integrated NPN switch, boost diode and sense resistor, the LT3474 cuts the external component count to a minimum. The high side sense allows a grounded cathode connection, easing wiring constraints. Both PWM and analog dimming are available with minor circuit modification; see the LT3474 data sheet for details.

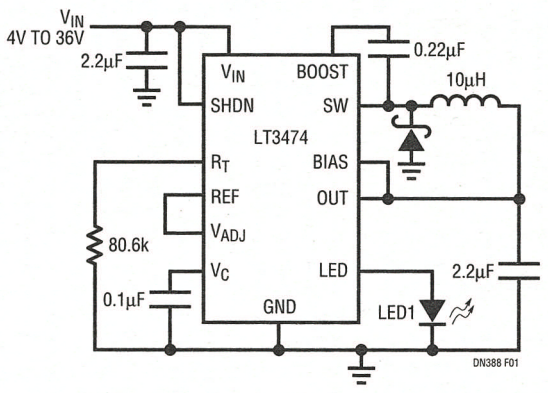


Figure 1. 4V-36V Input Voltage 1A LED Driver Requires Few Components

Driving LEDs from 12V_{AC} Input

The LT3474 directly regulates LED current, maintaining constant LED current over changing V_{IN}. The wide input range of the LT3474 allows direct connection to a rectified 12V_{AC} input. Using a small input capacitor, as shown in Figure 2, minimizes size. In this case, the LT3474 delivers nearly 1A of LED current as shown in Figure 3. Adding more capacitance to the input, as shown in Figure 4, holds the input voltage above the LED voltage. In this case, the LT3474 can deliver a constant LED current even with significant 120Hz ripple on the input as shown in Figure 5.

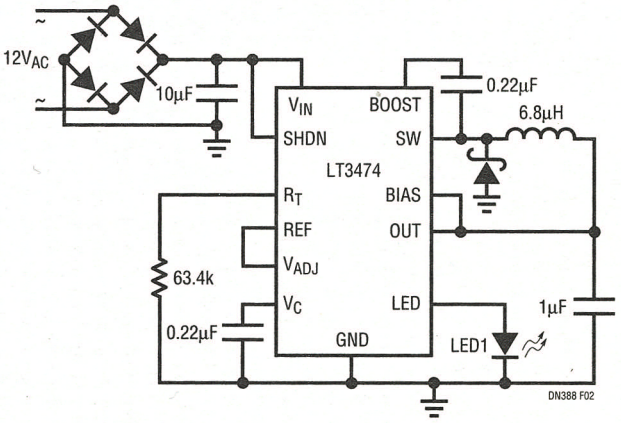


Figure 2. Using a Diode Bridge Allows the LT3474 to Drive an LED from a 12V_{AC} Input

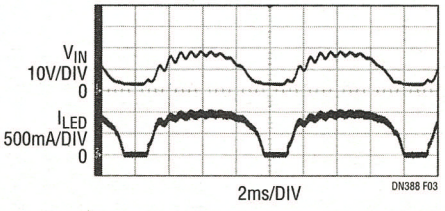


Figure 3. Using a 10µF Input Capacitance, the LT3474 Delivers Nearly 1A of LED Current with Smallest Board Size

Thermal regulation

The issue of heat management is at the core of many LED applications. A reliable solution maintains the longevity of the LED by keeping the LED junction temperature below the recommended limit. One answer to this problem is to mount massive heat sinks, wasting space and money. Figure 6 shows a better solution. The temperature of the LED is sensed by the thermistor mounted near the LED and is translated into a voltage signal to the V_{ADJ} pin. The V_{ADJ} pin reduces the current through the LED appropriately to meet the power derating specified by the Luxeon III Star manufacturer. Only slight modifications to the resistor values are required to adjust the circuit for use with other high brightness LEDs.

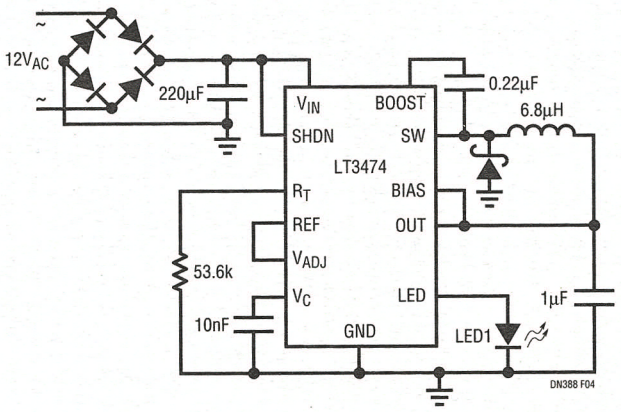


Figure 4. With a 220µF Input Capacitor, the LT3474 Supplies a Constant 1A Current to the LED

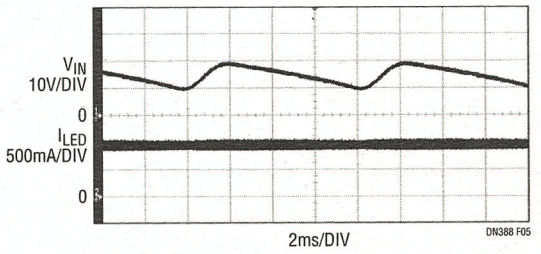


Figure 5. With a 220µF Input Capacitor, the LT3474 Delivers Constant 1A LED Current with Changing Input Voltage

Conclusion

High power white LEDs are fast becoming the lighting of choice in architectural, automotive, museum and avionic systems due to their efficiency, high quality light and long lifetimes. The LT3474 makes it easy to create compact, efficient, robust and versatile LED drivers from a variety of power supplies. Designers can now focus their time on creating imaginative new LED applications, instead of on LED drivers.

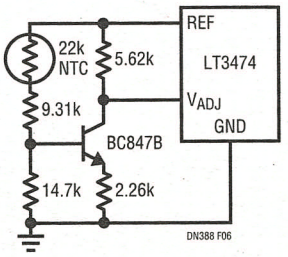


Figure 6. Compact, Economical Thermo-Regulating Circuit. The NTC and NPN, Mounted Close to the LED, Monitor the LED's Temperature

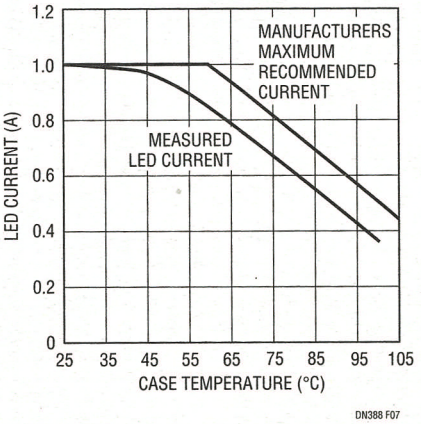


Figure 7. LED Current Safely Lies Within Specified Limits for the Luxeon III Star Power

Data Sheet Download

www.linear.com

For applications help,
call (408) 432-1900, Ext. 2759

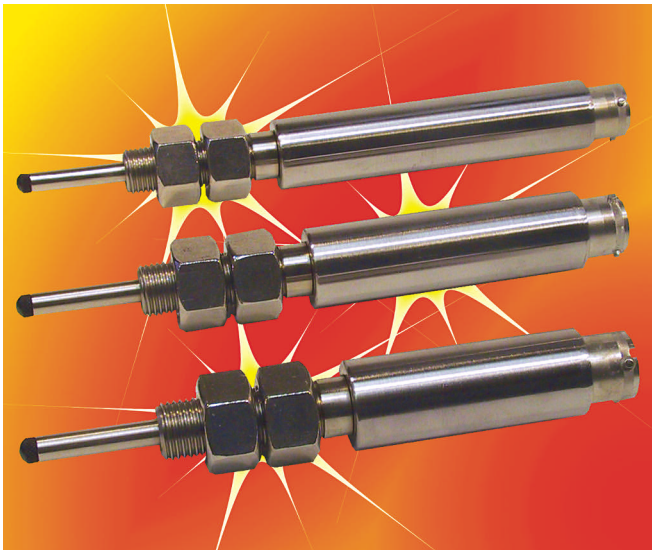
Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900 • FAX: (408) 434-0507 • www.linear.com

dn388f LT/TP 0406 409K • PRINTED IN THE USA

productroundup

SENSORS & TRANSDUCERS

LVDT-based position sensor can operate from PLC's 24V power supply



The LVDT (linear-variable-displacement-transducer)-based GHSE 750 series of 24V, spring-loaded position sensors operate from dc inputs at 15 to 24V and generate a precalibrated 0 to 10V-dc output. This output suits the device for most PLCs (programmable-logic controllers), digital indicators, ADCs, computer-based data processors, and QC data-collection systems. Ranging in size from 2.5 to 100 mm with a 19-mm-diameter sensor, the stainless-steel, hermetically sealed device provides long service life. Features include a 0.25% maximum-linearity error of full-scale output, coil windings sealed to IEC standard IP-68, and electrical termination through a glass-sealed axial connector. Units can operate from a PLC's 24V power supply. The GHSE 750 series costs $536.

Macro Sensors, www.macrosensors.com

MEMS-based sensors provide two or three axes of sensitivity

The xy-axis MMA6270Q, the xz-axis MMA6280Q, and the xyz-axis MMA7261Q MEMS-based (microelectromechanical-system) sensors extend the vendor's current offering from 1.5 to 10g. These three low-gravity accelerometers target electronic systems requiring detection of small changes in force resulting from fall, tilt, motion, positioning, shock, or vibration. Providing two or three axes of sensitivity, the devices can sense in lateral and perpendicular planes, eliminating the need for daughtercards. Features include selectable sensitivity for applications requiring various sensitivities for multiple applications and functions, a 500-µA current consumption, a 3-µA sleep mode, a 2.2 to 3.6V operating voltage, and a 1-msec power-up response. The MMA6270Q, MMA6280Q, and MMA7261Q cost $3.58, $3.85, and $4.43 (25,000), respectively.

Freescale Semiconductor, www.freescale.com

Current-sensing IC has a wide operating range

Featuring an 8 to 450V-dc operating range, the HV7800 high-side, current-sensing IC targets 12, 24, and 48V-dc power systems and 85 to 265V offline ac systems. Operating by sensing the voltage across an external resistor, the device then transmits the reading to the ground-reference circuit at a gain of one with a ±1% typical accuracy. The input-volt-

16-BIT MICROCONTROLLERS

Envision...16-bit Microcontrollers with 32-bit Performance and 8-bit Simplicity

16-bit PIC24 MCUs and dsPIC® Digital Signal Controllers

Unified 16-bit Architecture

- PIC24F, low-cost entry
- PIC24H, 40 MIPS high performance
- dsPIC30F/33F for seamless DSP integration

Low-Risk Design

- Easy step up from 8-bit MCUs
- Peripheral and Pin compatible families
- One development tool platform for all 8-bit and 16-bit MCUs and DSCs

Over 50 PIC24 Microcontrollers and dsPIC Digital Signal Controllers sampling today.
For data sheets, samples and pricing go to www.microchip.com/16bit

Explore. Design. Apply.

SEMINARS–16-bit MCU & DSC
Coming to over 100 cities worldwide

www.microchip.com/seminars

microchip DIRECT
www.microchipdirect.com

MICROCHIP
www.microchip.com/16bit

Microcontrollers • Digital Signal Controllers • Analog • Serial EEPROMs

productroundup

SENSORS & TRANSDUCERS

age range allows the IC to monitor current in telecom equipment, base stations, power-management systems, and LCD televisions with LED backlights. Available in SOT23-5 packages, the device complies with green and ROHS (reduction-of-hazardous-substances) specifications. The HV7800 costs 56 cents (1000).

Supertex, www.supertex.com

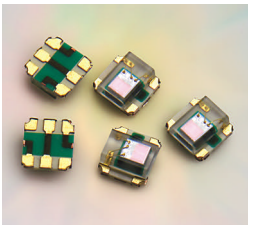
Thin digital accelerometer features smart functions

Embedding high performance and smart functions, the 1-mm-high, three-axis LIS3LV02DL digital accelerometer suits advanced motion-based applications in thin-profile, clamshell mobile phones. MEMS (microelectromechanical-system)-based accelerometers provide cost-effective motion-based user interfaces in mobile-system applications, including gesture recognition, motion-activated scrolling, and navigation on the phone display. Smart features include a free-fall and wake-up flag, adjustable bandwidth, direction detection, and a standard SPI/I^2C digital interface. Using the vendor's Thelma15 technology, the product provides ±2 and ±6g full-scale-acceleration ranges that can change by software command before and during operation. A robust design, tight offset tolerances, and high temperature stability provide a high immunity to vibration and a 10,000g shock resistance. Available in QFN-28 and LGA-16 packages, the LIS3LV02DL costs $4.

STMicroelectronics, www.st.com

Ambient-light sensor conserves battery power

Targeting mobile, consumer, commercial, and industrial devices, the APDS-9003 analog-output ambient-light photo sensor conserves battery power in portable devices by detecting the amount of ambient light and signaling the device when to turn on or off the display's backlight and keypad light. In large-panel displays, the device reduces LCD brightness to reduce eye glare and extend the life of the display. Performance features include operation over the 2.4 to 5.5V supply-voltage range, a 135-mA typical photo current at 100 lux for additional drive to control circuitry, and a −40 to +85°C temperature range. Measuring 1.6×1.5×0.55 mm, the sensor comes in a miniature, lead-free, surface-mount ChipLED-6 package. The APDS-9003 costs 24 cents.



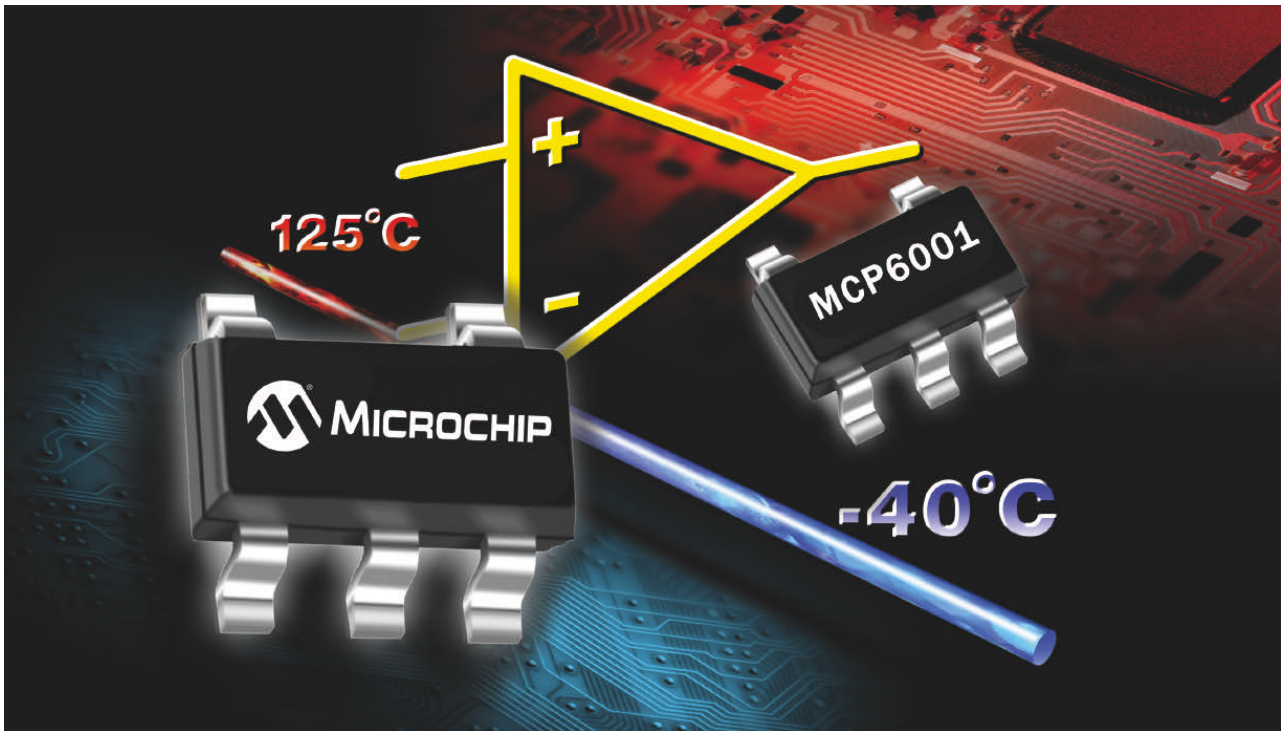
Avago Technologies, www.avagotech.com

EMBEDDED SYSTEMS

Hybrid embedded board features a four-DSP processing cluster

The first of a new line of hybrid embedded boards, the GT3U (GT-3U-cPCI) features an Altera Stratix II GX FPGA, a four-DSP-TS201S-TigerSharc processor cluster, and 1 Gbyte of DDR2 SDRAM. These processing clusters provide 14.4 GFLOPS of floating-point and 57.5 BOPS of 16-bit fixed-point processing power per board. Providing software support for the device, the vendor's tools include host-interface libraries, diagnostic utilities,

Low Power, Rail-to-Rail Input/ Output, Single Supply Op Amps



Select Standard Op Amps

Part #	GBWP	Iq Typical (µA)	Vos Max (mV)	Input Voltage Noise Density @ 1 kHz (nV/√Hz)	Operating Voltage (V)
MCP6041/2/3/4	14 kHz	0.6	3.0	170	1.4 – 5.5
MCP6141/2/3/4	100 kHz	0.6	3.0	170	1.4 – 5.5
MCP6231/2/4	300 kHz	20	5.0	52	1.8 – 5.5
MCP6241/2/4	550 kHz	50	5.0	45	1.8 – 5.5
MCP6001/2/4	1 MHz	140	4.5	28	1.8 – 5.5
MCP6271/2/3/4/5	2 MHz	170	3.0	20	2.0 – 5.5
MCP6281/2/3/4/5	5 MHz	445	3.0	16	2.2 – 5.5
MCP6291/2/3/4/5	10 MHz	1100	3.0	8.7*	2.4 – 5.5
MCP6021/2/3/4	10 MHz	1000	0.5	8.7*	2.5 – 5.5

* Value is typical at 10 kHz

Now available for purchase on....
microchip DIRECT
www.microchipdirect.com
One-stop shopping for MCUs, digital signal controllers, analog and serial EEPROMs.

- Select devices available in PDIP, SOIC, MSOP, TSSOP, SOT-23, and SC-70
- Select devices offer a Chip Select pin for additional power savings
- The MCP62X5 offers dual amplifiers with a Chip Select pin in an 8-pin package
- Order free samples and download the free FilterLab® Active Filter Design Tool at www.microchip.com

Now Pb-free!

MICROCHIP
www.microchip.com/OpAmps

Microcontrollers • Digital Signal Controllers • Analog • Serial EEPROMs

and configuration tools. Also available are the TS-Lib optimized libraries for TigerSharc; a board-support package for Gedae; and third-party tools supporting the hybrid embedded boards, including Analog Devices' VisualDSP++ and targets for the Mathworks' Matlab and Simulink. RTOS support includes Analog Devices' VDK (VisualDSP kernel) and Enea's OSEck. The commercial and ruggedized versions of the GT3U cost $9995 and $14,995, respectively for the 512-Mbyte DDR2 SDRAM options.

BittWare Inc, www.bittware.com

Upgraded design provides faster PowerPC

Improved connectivity and performance for the PowerNode3+ come from two PCI-mezzanine-card sites, a 1-Mbyte internal L2 cache, VME 2eSST with 320-Mbps peak-bandwidth capability, and optional serial RapidIO PMC switch fabric. The device also features two PowerPC 7448s running at 1.4 GHz. Several versions are available, including a rugged version for harsh environments. A unique shared-memory architecture supports LynxOS, VxWorks, and Linux SMP. The PowerNode3+ costs $5154.

Thales Computers, www.thalescomputers.com

I/O module monitors and controls SSRs

Expanding on the 2600 series of smart I/O modules, the 2652 monitors and controls eight SSRs (solid-state relays) using a Category 5 patch cable connecting to a 2601 communication module. Designers can populate each SSR socket with an ac-in or -out or dc-in or -out SSR. To minimize errors from electromechanical-switch bounce, the device uses a software-debouncer filter for the input SSRs. As an output, the client can explicitly control the SSR, or the SSR can operate as a PWM output with a rate and duty cycle that the client specifies. Five independent interlock circuits allow external circuitry, including an emergency stop switch, to de-energize an output SSR.

Sensoray, www.sensoray.com

Universal tool supports Freescale RS08 devices

Targeting Freescale microcontrollers, the inDart-One universal tool supports RS08 devices for programming and debugging. This family features a stripped-down S08 core and a pin-count reduction aiming at cost-effective embedded-system applications. A robust structure provides high resistance to electrical shocks, suiting the device for production programming in heavy production environments. In addition, the tool allows simultaneous programming of 32 devices from one host PC over a USB 2.0 connection. The inDart-One costs $399.

SofTec Microsystems, www.softecmicro.com

Rugged switcher/router card supports multiple management interfaces

The rugged 3U CompactPCI SCP/DCP-681 Compact SwitchBlade Gigabit Ethernet switcher/router card supports CLI, Telnet, Web, and SNMP management interfaces. These interfaces configure a set of protocols including PBIT (Power-up Built-In Test), IBIT (Initiated Built-In Test), CBIT (Continuous Built-In Test), Layer 2 protocol, Layer 3 (Internet Protocol Version 4/Version 6) protocols, multicasting, quality of service, and security. The device also features the secure-memory-erase function. SCP/DCP-681 Compact SwitchBlade costs $9100.

Curtiss-Wright Controls Embedded Computing, www.cwcembedded.com

EDN productmart

This advertising is for new and current products.

EDN ADVERTISER INDEX

This index is provided as an additional service. The publisher does not assume any liability for errors or omissions. For immediate information on products and services, go to Reader Service under Tools & Service at www.edn.com.

STATS Uses same CSMA/CA method as the original 802.11 / Employs 52-subcarrier OFDM modulation

Wireless protocol lags initial expectations

When the IEEE ratified the IEEE 802.11a specification in 1999, many technology providers and observers felt it had a bright future. The 802.11a spec touted raw data rates as high as 54 Mbps, employed the relatively spectrum-uncluttered, 5-GHz FCC Part 15 unlicensed frequency band, and offered 12 nonoverlapping channels. IEEE 802.11b, in contrast, broadcasted on the same 2.4-GHz spectrum that common office and household appliances inhabit, could support only 11-Mbps-peak raw data rates, and used 14 overlapping channels.

Unlike 802.11a, however, 802.11b was backward-compatible with the initial 1- and 2-Mbps 802.11 standard and with its Lucent-developed WaveLAN foundation protocol. Reliance on 2.4 GHz increased the probability of interference, but it also gave 802.11b longer range than 802.11a. A two-year lag between 802.11a-spec ratification and shipping products gave 802.11b an early market lead. And the mid-2003 ratification of 802.11b backward-compatible 802.11g, which also touted 54-Mbps-peak raw data rates, resigned 802.11a to niche status.

Yet, 802.11a lives on; Microsoft, for example, recommends using 802.11a to wirelessly stream high-definition video to its Xbox 360 game console to minimize the probability of packet-delaying and -dropping interference. Many laptop computers' integrated Wi-Fi transceivers, along with many USB, Category 5, and PC Card adapters, support a, b, and g. And the pending 802.11n standard supports optional backward-compatibility with both 2.4- and 5-GHz-based protocols.—by Brian Dipert

OrCAD PCB Designer lets you customize reports on demand

Scalable, cost-effective solution for complex PCB designs

Producing customized reports is just one of the many tasks made easy with OrCAD® PCB Designer. Here are some others:

- Adding or customizing drill tolerances, symbols, and characters
- Routing power and ground to split power planes
- Quickly creating the fanout for dense, high-pin-count devices
- Placing critical components to optimize logical connections

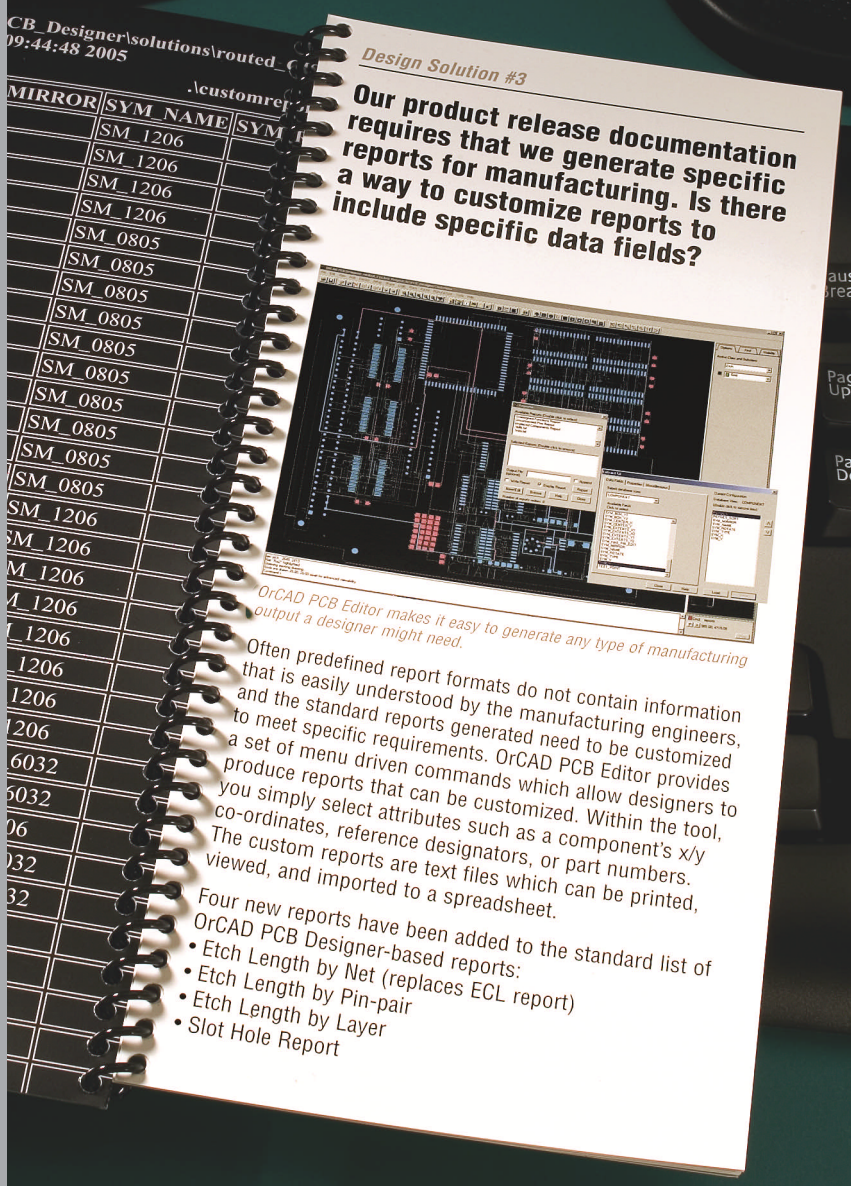
OrCAD PCB Designer suites offer a complete front-to-back PCB design solution based on powerful technology:

- OrCAD Capture® schematic entry
- OrCAD PCB Editor place-and-route (based on Cadence® Allegro® technology)
- SPECCTRA® for OrCAD autorouter (based on Cadence Allegro technology)

You can further enhance productivity by adding optional PSpice® A/D for circuit simulation or by adding OrCAD Signal Explorer (based on Cadence Allegro technology) for signal integrity and topology exploration.

We've assembled some of your most common PCB design issues into a booklet, the OrCAD PCB Designer Solutions Guide. Get your FREE copy today!

Get your free solutions guide
Visit us at
www.ema-eda.com/PCBDesignerGuide
or call us at 800.813.7288



OrCAD®

EMA Design Automation™
ema-eda.com

Get in touch with any application.

PSoC®–based Capacitive Touch Sensing

Simple. Flexible. Integrated. *CapSense.* Capacitive sensing replaces mechanical buttons, switches, touchpads, sliders, and proximity detectors in systems from cell phones and cars to notebook PCs, white goods and industrial applications. Immune to environmental wear-and-tear, Cypress's cost-effective CapSense solution leverages the flexibility of our configurable PSoC® mixed-signal array and brings elegance, economy and functionality to your designs.

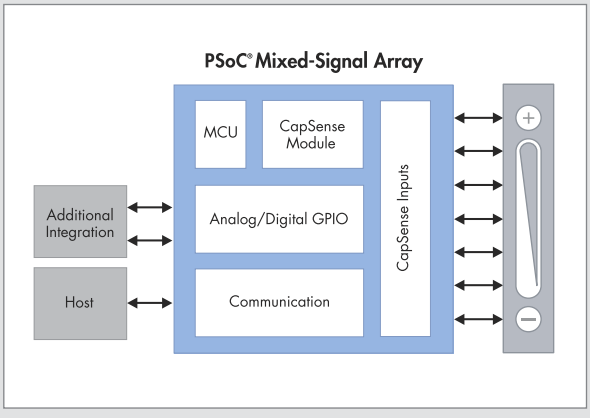
HOT SPEC *Cypress's CapSense solution integrates multiple buttons/sliders/touchpads on a single chip, using no external resistors or capacitors*

- *Flexible implementation vs. hard-coded ASICs or fixed-function modules*
- *Easy serial communications with I²C, SPI and USB interfaces*
- *Easy-to-use PSoC tools provide system-level embedded design with quick time-to-market*

FOR MORE INFORMATION

For a free online or face-to-face seminar with PSoC CapSense experts, visit www.cypress.com/touch

CYPRESS CAPSENSE CIRCUIT DIAGRAM



PSoC® CapSense implementation with two buttons and a slider using a single PSoC device.

CapSense Device Selector Guide

Device	Resources	Available Package
CY8C21x34	8 KB Flash, 512 B RAM, I²C, SPI	16-SOIC, 20-SSOP, 28-SSOP, 5x5 mm 32-MLF
CY8C24x94	16 KB Flash, 1 KB RAM, I²C, Full-speed USB, SPI	8x8 mm 56-MLF

CYPRESS PERFORM